

Thorpe-1 SWG SOVP Logic Schematics

THP1H-8
VER 8.04
Dec/15/2015

BASE LOGIC :
Thorpe-1 SWG SVT-R VER 7.08 Sep/14/2015

1.TITLE PAGE	36.GBE MAGNETICS	
2.EC HISTORY	37.RJ45 CONNECTOR	
3.CPU(1/16) : DDI/EDP	38.N16S-LP(1/6) : PEG I/F	
4.CPU(2/16) : DDR CHANNEL-A	39.N16S-LP(2/6) : DIGITAL OUT I/F	
5.CPU(3/16) : DDR CHANNEL-B	40.N16S-LP(3/6) : VRAM I/F	
6.CPU(4/16) : MISC/JTAG	41.N16S-LP(4/6) : GPIO	
7.CPU(5/16) : LPC/SPI/SMBUS/C-LINK	42.N16S-LP(5/6) : POWER	
8.CPU(6/16) : LPSS/ISH	43.N16S-LP(6/6) : GND	
9.CPU(7/16) : AUDIO/SDXC	44.VRAM CHANNEL-A	
10.CPU(8/16) : PCIE/USB/SATA	45.MEMORY TERMINATION	
11.CPU(9/16) : CSI-2/EMMC	46.PCIE M.2 (NGFF) CARD SLOT	
12.CPU(10/16) : CLOCK SIGNALS	47.SD/AUDIO CONNECTOR I/F	
13.CPU(11/16) : SYSTEM PM	48.BLANK	
14.CPU(12/16) : CPU POWER (1/2)	49.BLANK	
15.CPU(13/16) : CPU POWER (2/2)	50.AUDIO ALC3245	
16.CPU(14/16) : PCH POWER	51.AUDIO HP JACK DETECT	
17.CPU(15/16) : GND	52.AUDIO JACK SENSE	
18.CPU(16/16) : CFG/RESERVED	53.BLANK	
19.XDP CONNECTOR	54.AUDIO SPEAKER	
20.RTC BATTERY	55.AUDIO BEEP	
21.SPI FLASH	56.BLANK	
22.DDR4 BASE MEMORY CH-A (1/2)	57.DOCKING CONNECTOR	
23.DDR4 BASE MEMORY CH-A (2/2)	58.MEC1653(1/3)	
24.DDR4 SO DIMM CHANNEL-B (1/2)	59.MEC1653(2/3)	
25.DDR4 SO DIMM CHANNEL-B (2/2)	60.MEC1653(3/3)	
26.LCD/USB/LID/MIC/CAMERA/PWR SW	61.KEYBOARD/TRACK POINT	
27.DISPLAY PORT CONNECTOR	62.TOUCH PAD/FPR/SCR	
28.DDI DEMULTIPLEXER	63.FAN CONNECTOR	
29.DDI DEMUX/HDMI LEVEL SHIFTER	64.APS G-SENSOR	
30.HDMI CONNECTOR	65.DISCRETE TPM 1.2	
31.M.2 SATA/PCIE SSD CARD SLOT	66.SMBUS SWITCH/LPC DEBUG PORT	
32.USB POWER/CONN	67.THINK ENGINE-2(1/2)	
33.BLANK	68.THINK ENGINE-2(2/2)	
34.GBE JACKSONVILLE	69.DC-IN	
35.GBE LAN SWITCH	70.BATTERY INPUT	
		71.BATTERY CHARGER(BQ24780S)
		72.CHARGER SELECTOR
		73.BLANK
		74.DC/DC VCC5M/VCC3M (TPS51285B)
		75.DC/DC IMVP8 CONTROLLER(NCP81208)
		76.DC/DC VCCCPUCORE(NCP81382)
		77.DC/DC VCCGFXCORE_I(NCP81382)
		78.DC/DC VCCSA(NCP81382)
		79.DC/DC VCCGFXEXT(NCP81210)
		80.DC/DC VCCCPUIO(NB682)
		81.DC/DC VCC1R0_SUS(BD91364BMUU)
		82.LOAD SW VCCST & VCCSTG
		83.DC/DC VCC1R2A(SN1409027)
		84.DC/DC VCC0R6B(TPS51206)
		85.DC/DC VCC2R5A(TLV62080)
		86.DC/DC VCC1R8_SUS(BU90004GWZ)
		87.DC/DC VCCPCHCORE(NB682)
		88.DC/DC VCCEDRAM(NB682)
		89.DC/DC VCCEOPIO(NB682)
		90.DC/DC VCCGFXCORE_D(TPS51219)
		91.DC/DC VCC1R35VIDEO(SN1409027)
		92.BLANK
		93.LOAD SW PCH SUS/TRACK POINT
		94.LOAD SW LAN
		95.LOAD SW VIDEO
		96.LOAD SW B
		97.LOAD SW WWAN & WLAN
		98.BLANK
		99.PTH FOR SCREW HOLES

EC HISTORY

CS15 THP1H-8
(BASE LOGIC : Thorpe-1 SWG SVT-R VER 7.08 Sep/14/2015)

VER.8.00 11/11/2015 APPLIED THP1_SWG_SOVP_EC001-005
VER.8.01 11/12/2015 APPLIED THP1_SWG_SOVP_EC006,007
VER.8.02 11/16/2015 APPLIED THP1_SWG_SOVP_EC008,010
VER.8.03 11/20/2015 APPLIED THP1_SWG_SOVP_EC011-014
VER.8.04 12/15/2015 APPLIED THP1_SWG_SOVP_EC015,016

TABLE: Chip Capacitor Thermal Characteristics

		Code
-55 to 150degC -55 to 125degC	+/-30ppm/degC +/-30ppm/degC	NPO C0G
-55 to 125degC -55 to 105degC -55 to 85degC	+/-15% +/-22% +/-15%	X7R X6S X5R

TABLE: Chip Capacitor Tolerance

Tolerance	Code
+/-0.25pF +/-0.5pF	C D
+/-5% +/-10% +/-20% +80/-20%	J K M Z

TABLE: Chip Part Dimension

Size [mm]	mm Size Code	Inch Size Code
0.40 x 0.20 0.60 x 0.30 1.00 x 0.50 1.60 x 0.80 2.00 x 1.25 2.00 x 1.60 2.50 x 2.00 3.20 x 1.60 3.20 x 2.50 4.50 x 1.60 4.50 x 2.50 4.50 x 3.20 5.00 x 2.50 6.40 x 3.20	0402 0603 1005 1608 2125 2016 2520 3216 3225 4516 4525 4532 5025 6432	01005 0201 0402 0603 0805 0806 1008 1206 1210 1806 1810 1812 2010 2512

↑
LOGIC

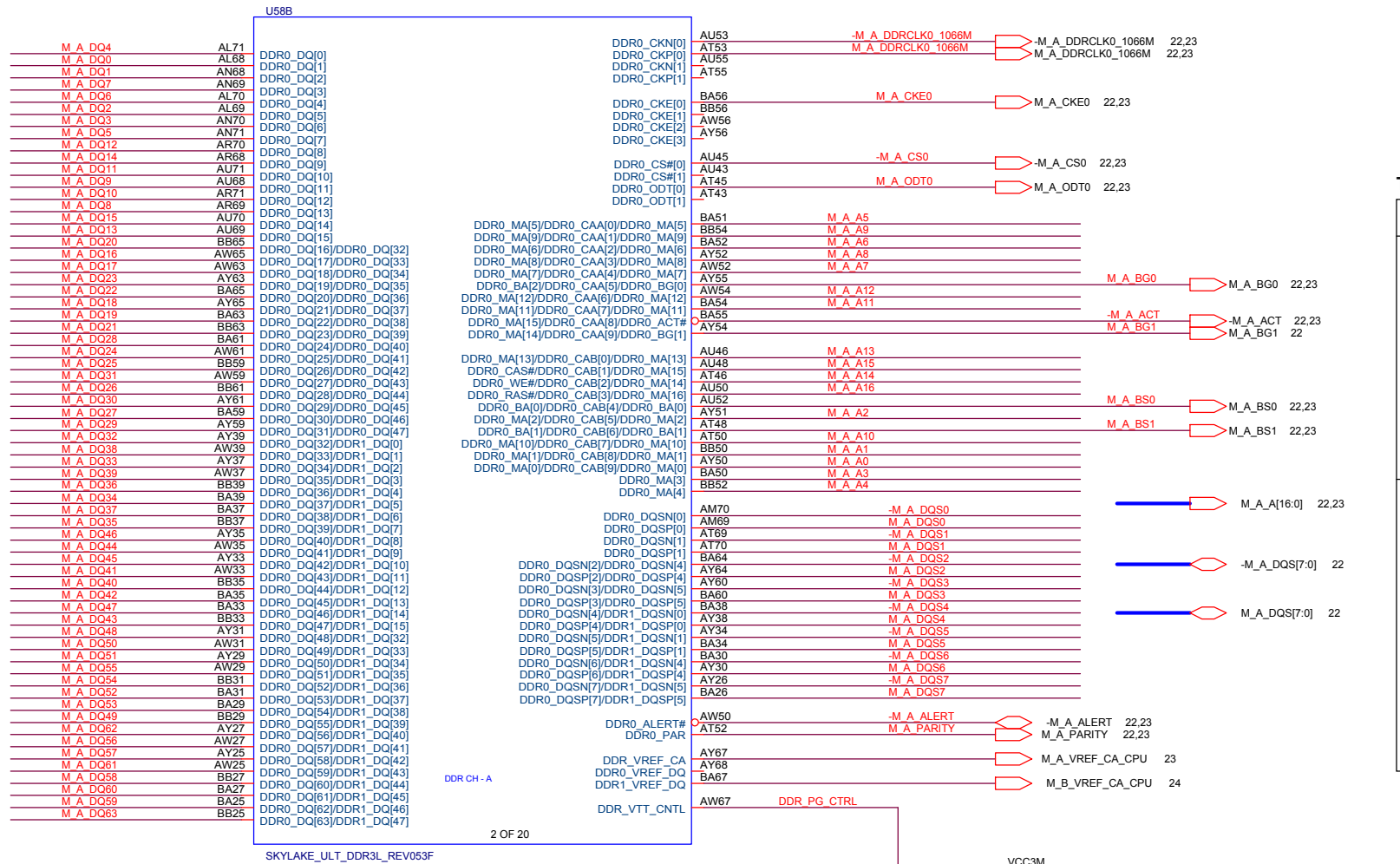


Project Name : THP1_SWG_SOVP		Title : EC HISTORY	
Size : C	Document Number :		Rev : 8.04
Date: Tuesday, December 15, 2015		Sheet : 2 of 99	

TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
	AY59	DDR0_DQ[31]	DDR0_DQ[47]
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
	BB25	DDR0_DQ[63]	DDR1_DQ[47]

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TABLE

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

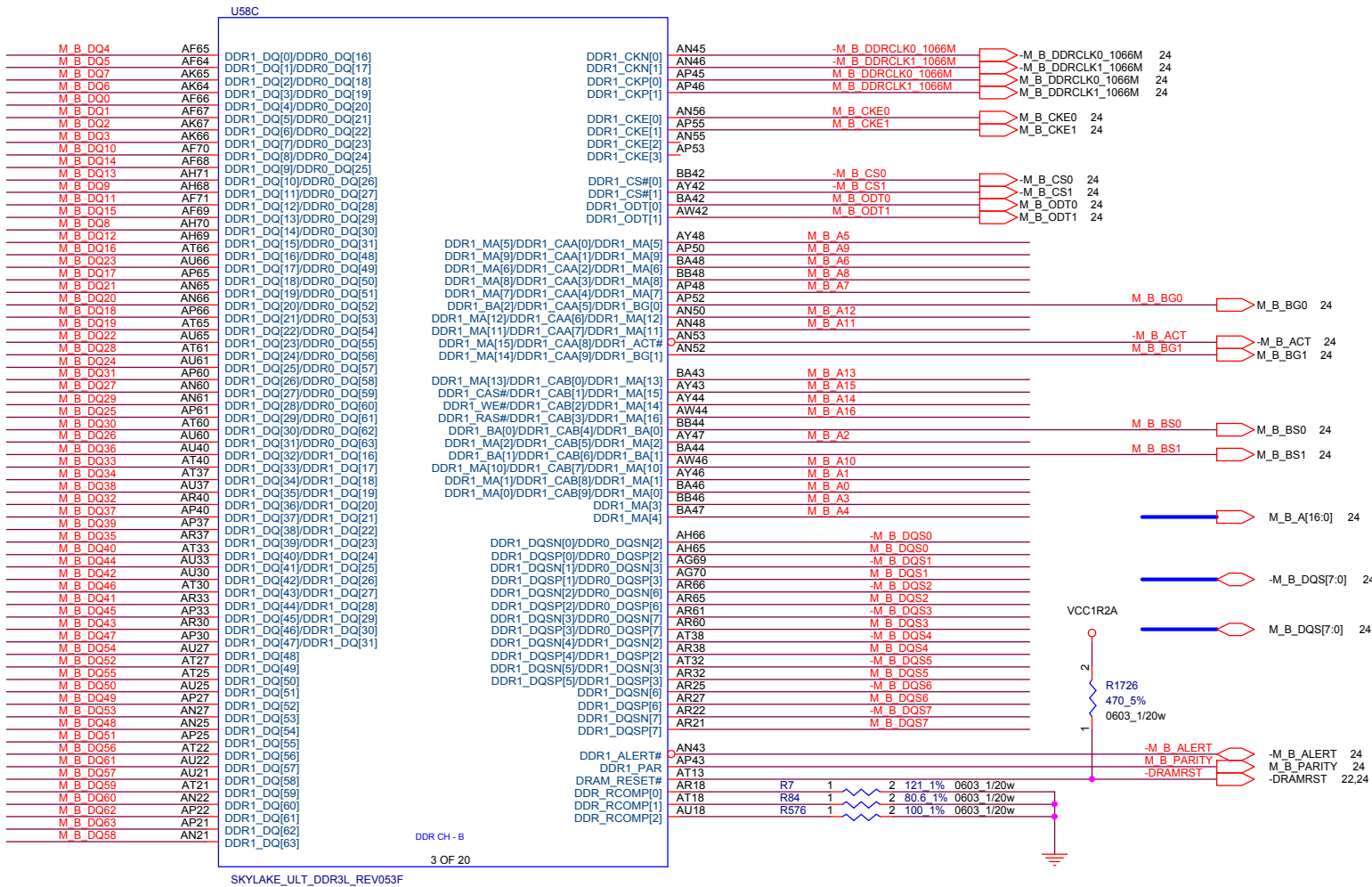
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TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC



TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC

lenovo

TABLE : Functional Strap

SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

TABLE : Functional Strap

SPI0_MISO (JTAG ODT Disable)	
HIGH	Enabled (Default)
LOW	Disabled

TABLE : Functional Strap

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

← LOGIC

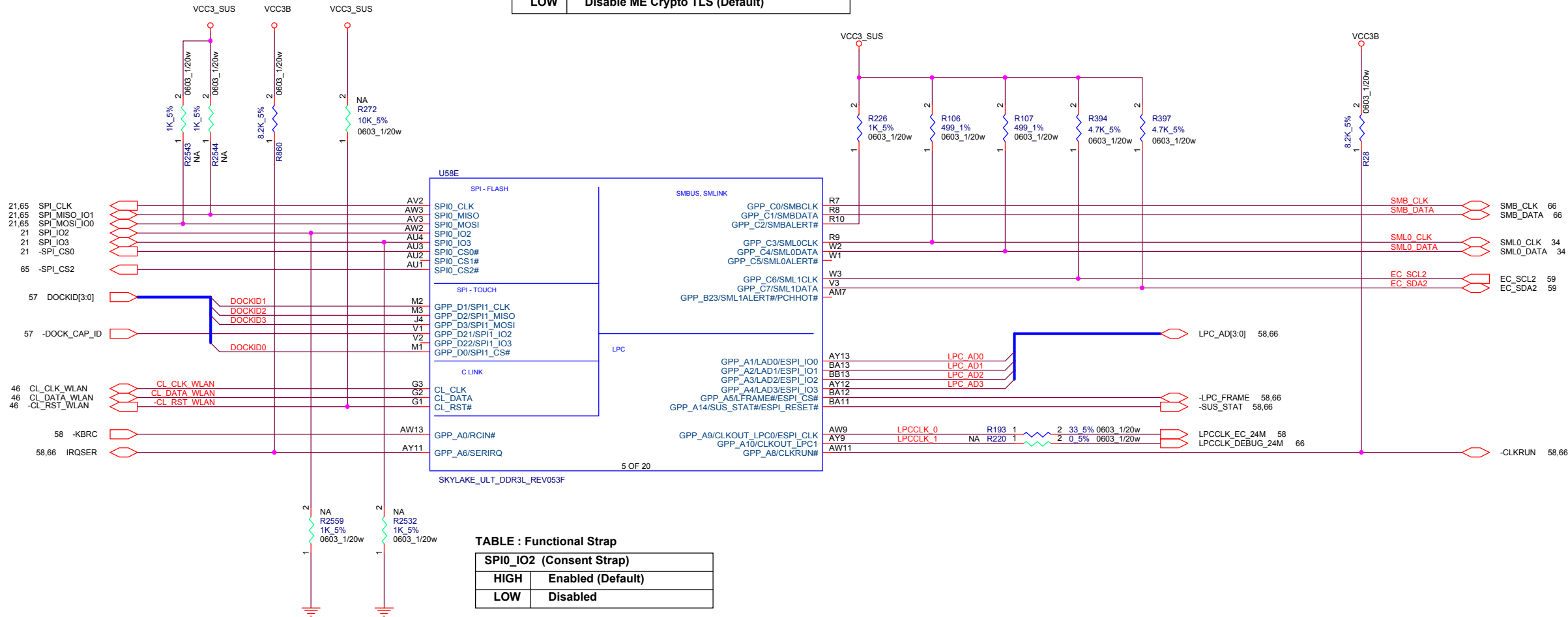


TABLE : Functional Strap

SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

TABLE : Functional Strap

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled



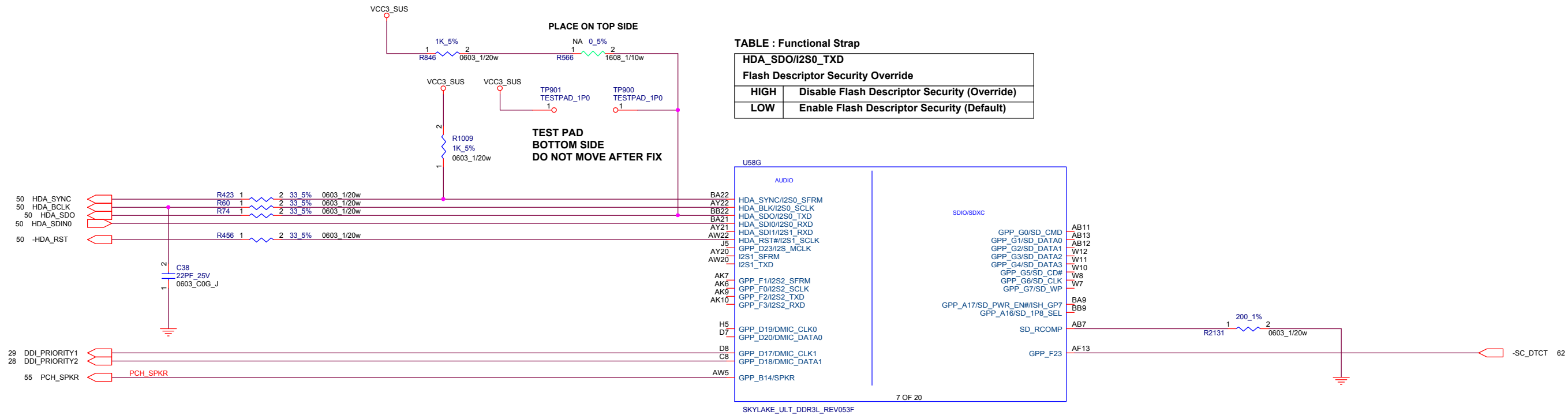


TABLE : Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

TABLE : Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

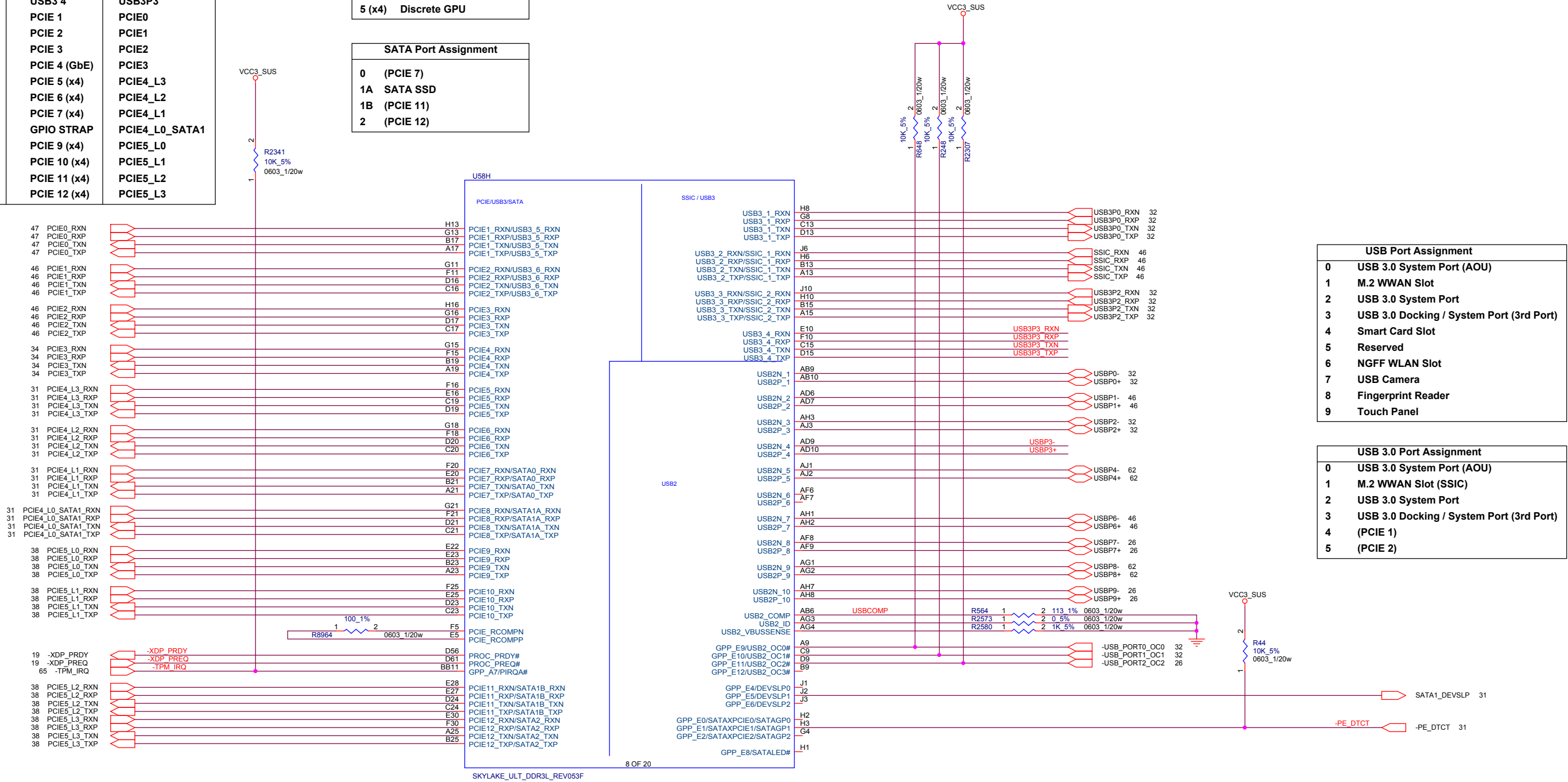
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Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC	SSIC	SSIC
Port 3	USB3 3	USB3 3	USB3P2
Port 4	USB3 4	USB3 4	USB3P3
Port 5	USB3 5/PCIE 1	PCIE 1	PCIE0
Port 6	USB3 6/PCIE 2	PCIE 2	PCIE1
Port 7	PCIE 3 (GbE)	PCIE 3	PCIE2
Port 8	PCIE 4 (GbE)	PCIE 4 (GbE)	PCIE3
Port 9	PCIE 5 (GbE)	PCIE 5 (x4)	PCIE4_L3
Port 10	PCIE 6	PCIE 6 (x4)	PCIE4_L2
Port 11	PCIE 7/SATA 0	PCIE 7 (x4)	PCIE4_L1
Port 12	PCIE 8/SATA 1A	GPIO STRAP	PCIE4_L0_SATA1
Port 13	PCIE 9 (GbE)	PCIE 9 (x4)	PCIE5_L0
Port 14	PCIE 10 (GbE)	PCIE 10 (x4)	PCIE5_L1
Port 15	PCIE 11/SATA 1B	PCIE 11 (x4)	PCIE5_L2
Port 16	PCIE 12/SATA 2	PCIE 12 (x4)	PCIE5_L3

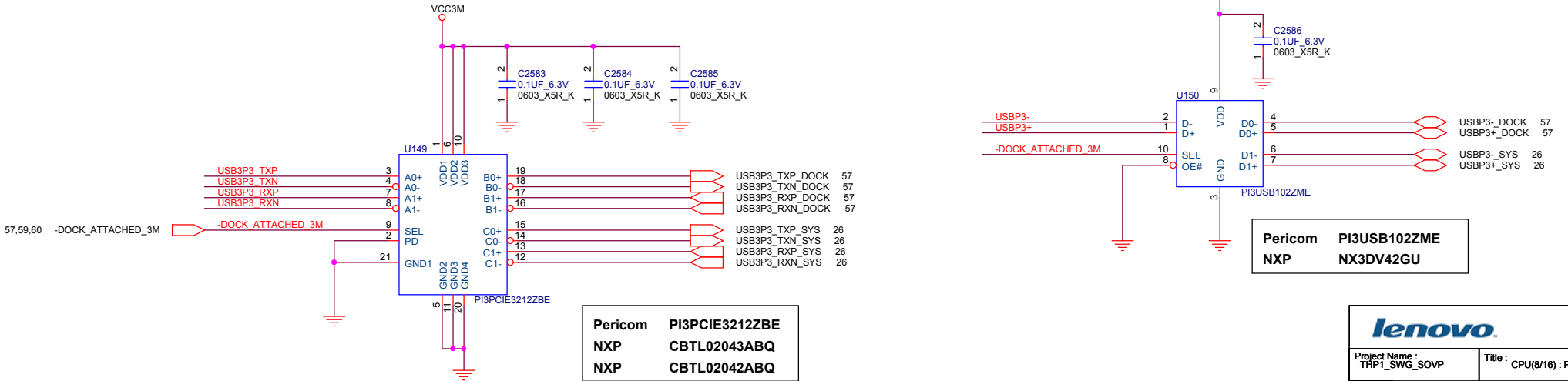
PCIe Port Assignment	
0	Media Card Controller
1	M.2 WLAN Slot Port 1
2	M.2 WLAN Slot Port 0
3	GbE PHY
4 (x4)	PCIe SSD
5 (x4)	Discrete GPU

SATA Port Assignment	
0	(PCIE 7)
1A	SATA SSD
1B	(PCIE 11)
2	(PCIE 12)



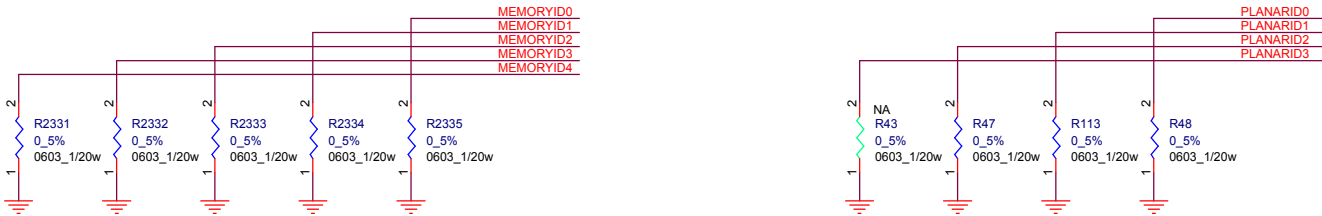
USB Port Assignment	
0	USB 3.0 System Port (AOU)
1	M.2 WWAN Slot
2	USB 3.0 System Port
3	USB 3.0 Docking / System Port (3rd Port)
4	Smart Card Slot
5	Reserved
6	NGFF WLAN Slot
7	USB Camera
8	Fingerprint Reader
9	Touch Panel

USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	M.2 WWAN Slot (SSIC)
2	USB 3.0 System Port
3	USB 3.0 Docking / System Port (3rd Port)
4	(PCIE 1)
5	(PCIE 2)



TABLE

MEMORYID[4..0]	U125, U126, U127, U128			
00000b	Micron	MT40A512M16HA-083E:A	8Gbit SDP	4GB
00001b	Micron	MT40A1G16HBA-083E:A	16Gbit DDP	8GB
00010b	Samsung	K4A8G165WB-BCPB	8Gbit SDP	4GB
00011b	SK Hynix	T.B.D.	8Gbit DDP	4GB
00100b	SK Hynix	T.B.D.	8Gbit SDP	4GB
11111b	NO_ASM		No Soldered Memory	



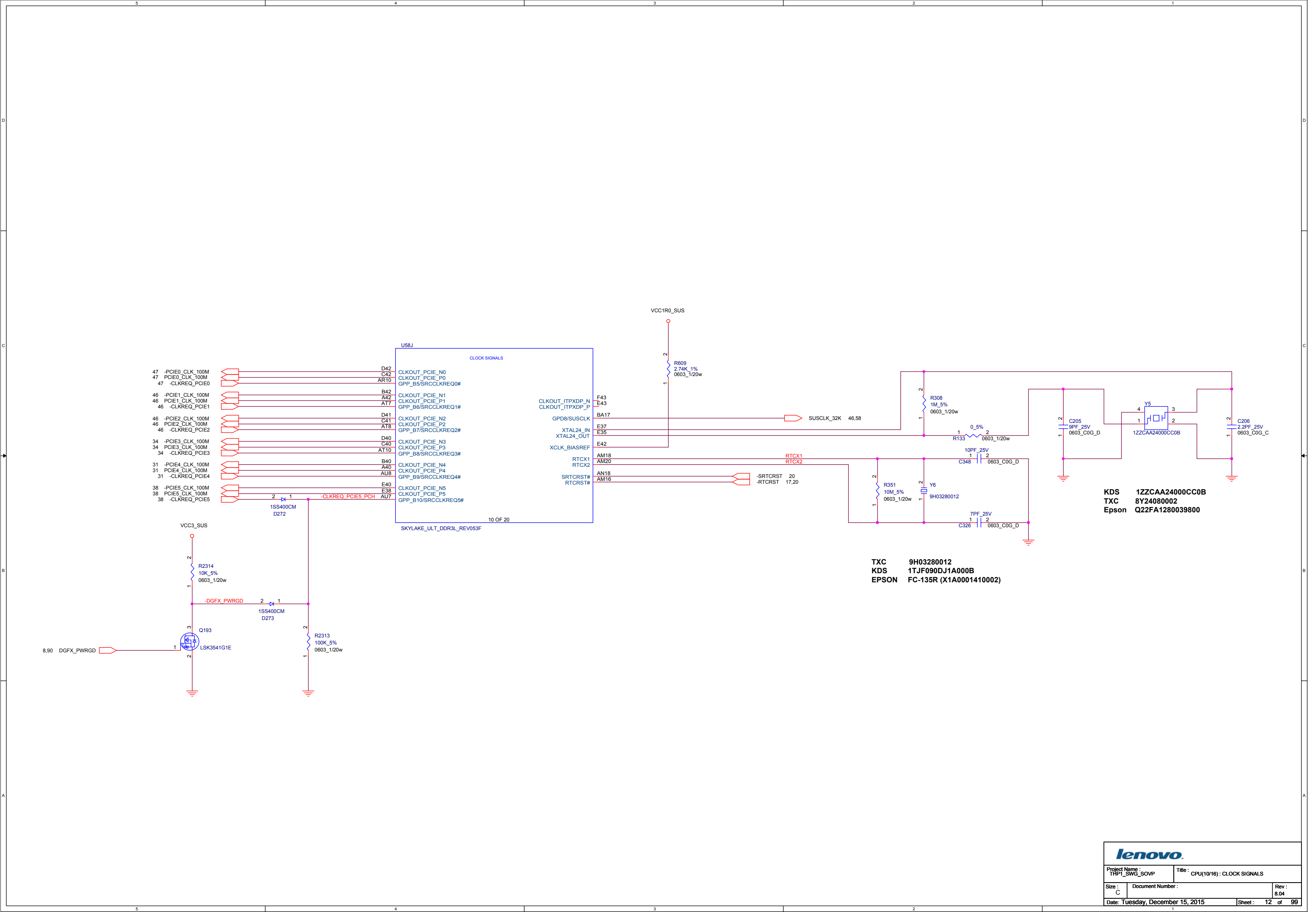
TABLE

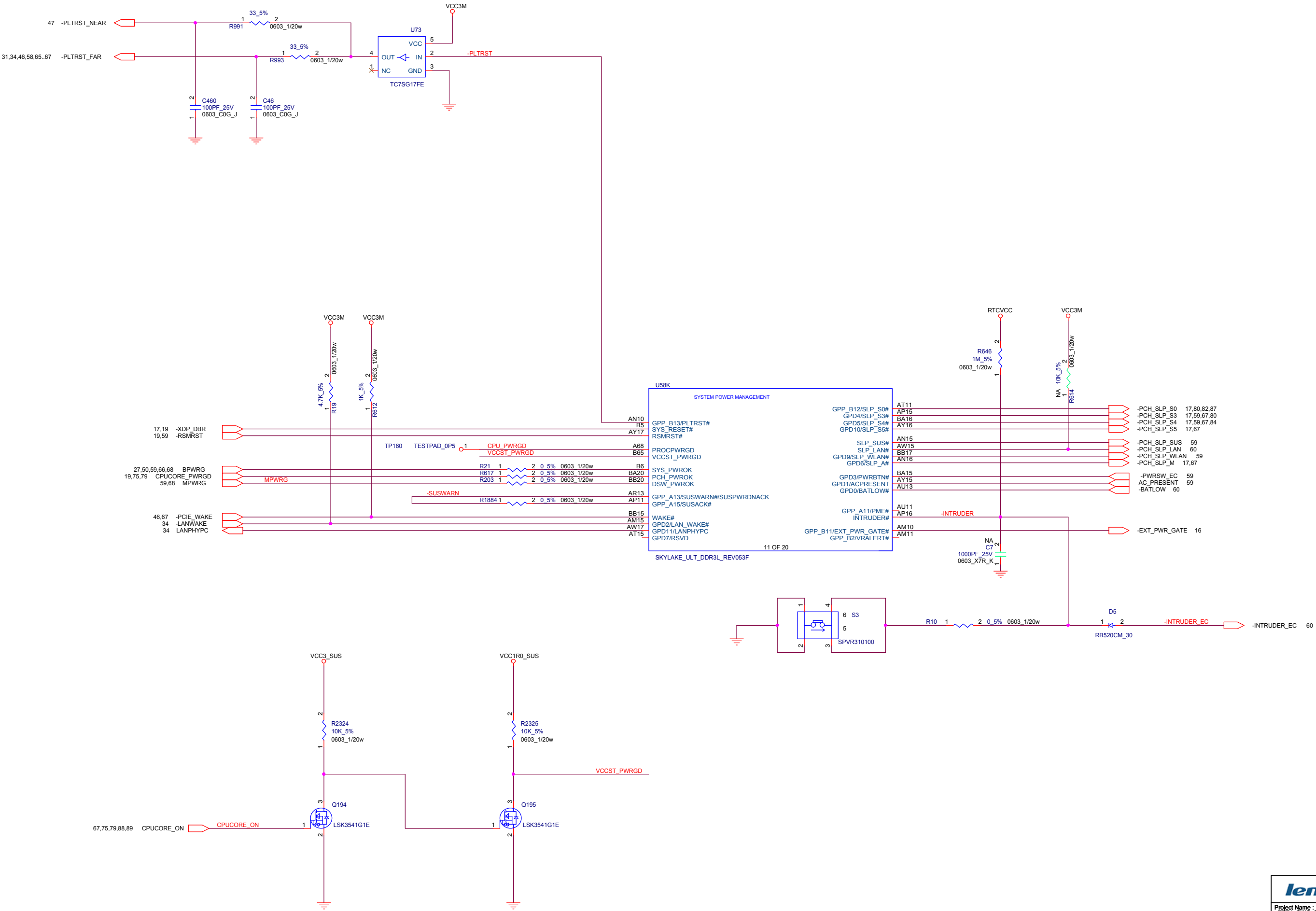
LEVEL	PLANAR ID			
	3	2	1	0
	R43	R47	R113	R48
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

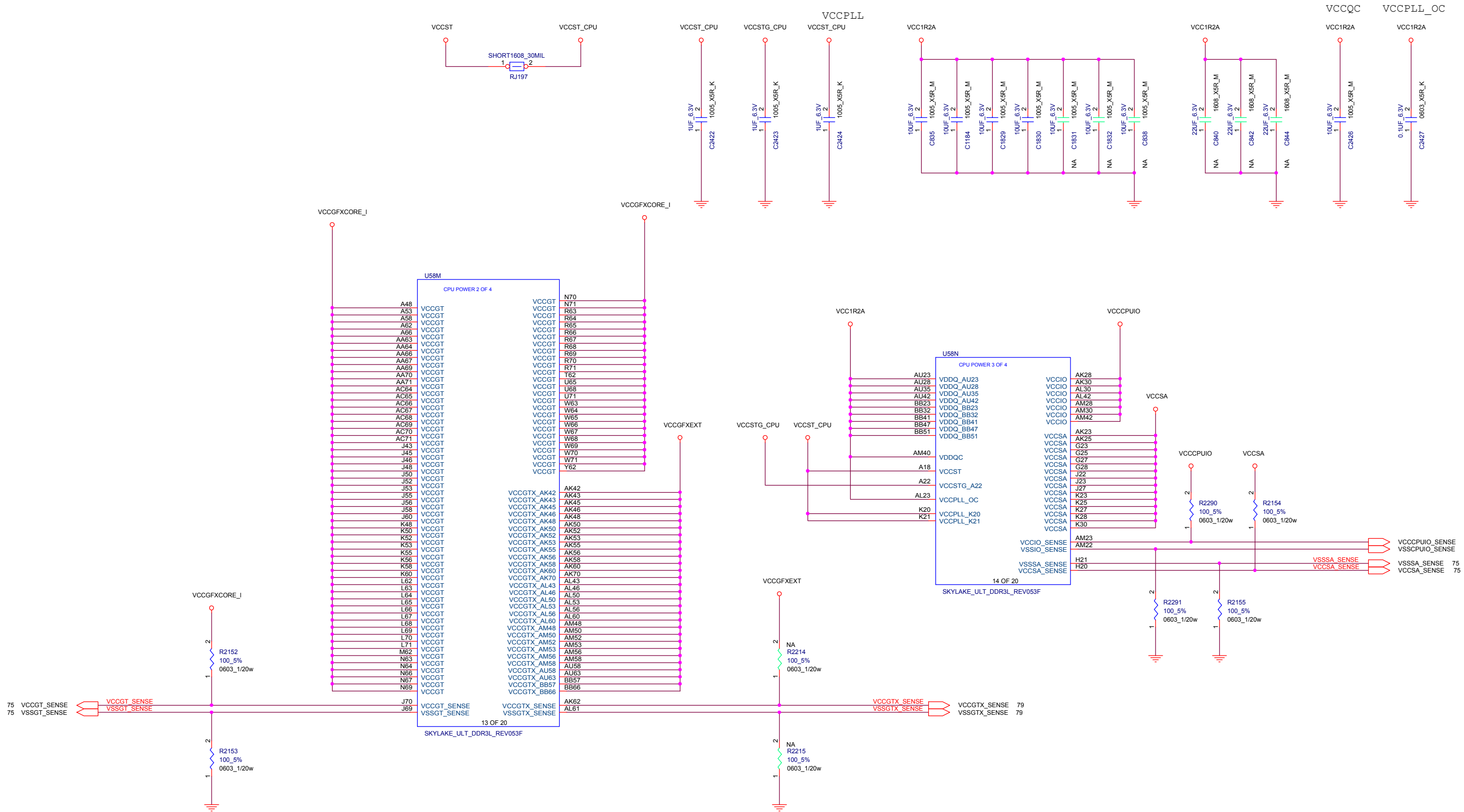
TABLE

LEVEL	PLANARID[3..0]
PDV	0000B
SDV	0001B
FVT	0010B
ME SIT	0011B
SIT	0100B
SIT-R	0101B
SVT	0110B
SVT-R	0111B
SOVP	1000B









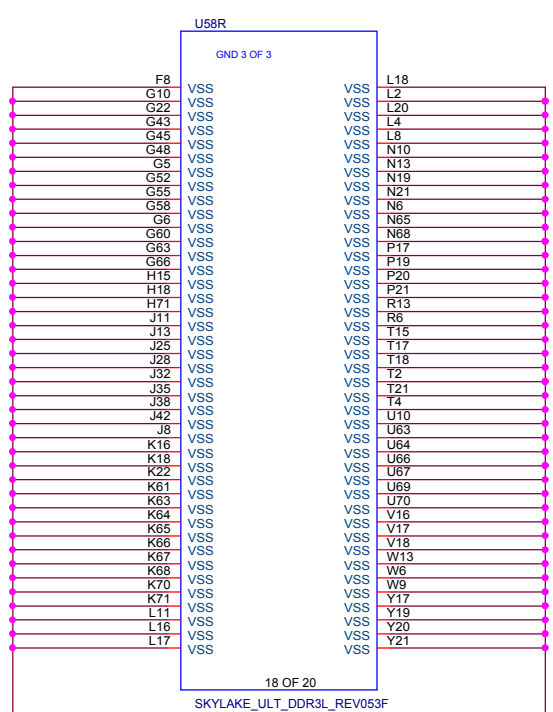
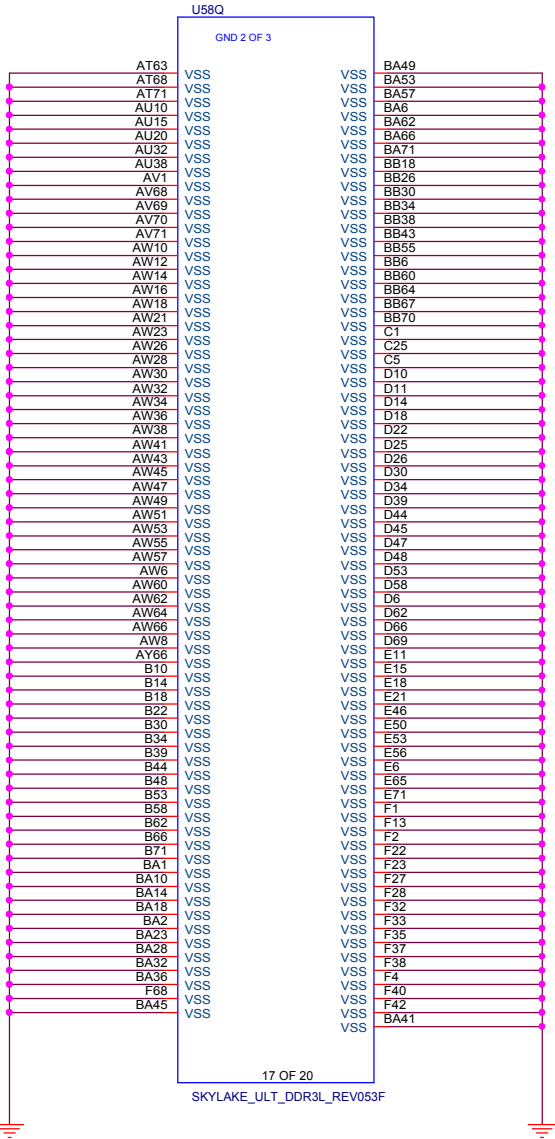
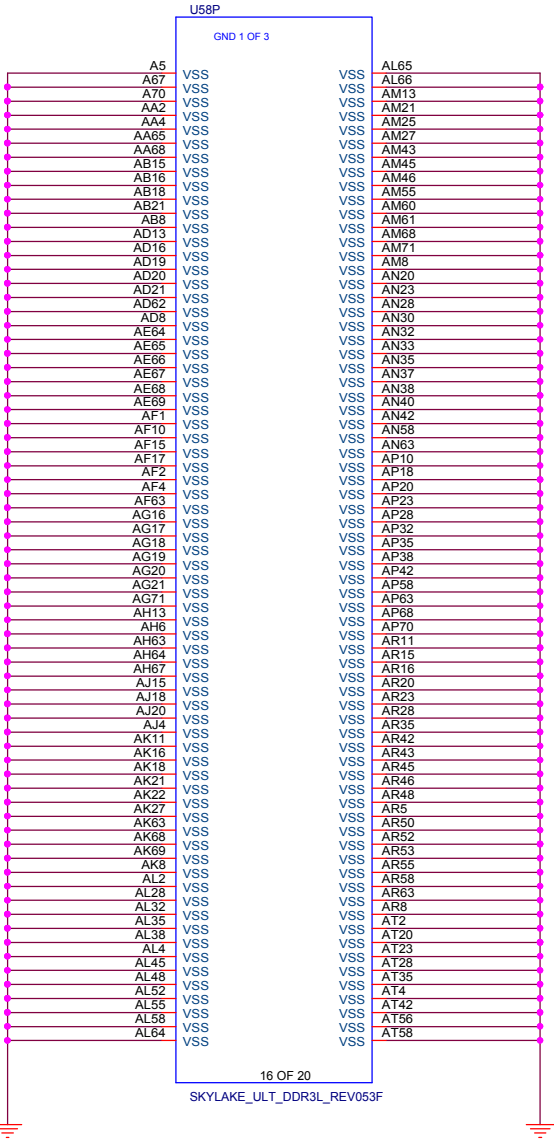
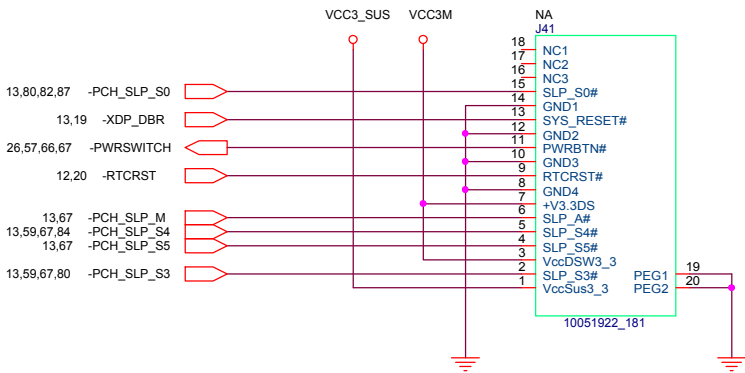
Project Name : THP1_SWG_SOVP Title : CPU(13/16) : CPU POWER (2/2)

Size : C Document Number : Rev : 8.04

Date : Tuesday, December 15, 2015 Sheet : 15 of 99

Date: Tuesday, December 15, 2015	Sheet : 16 of 99
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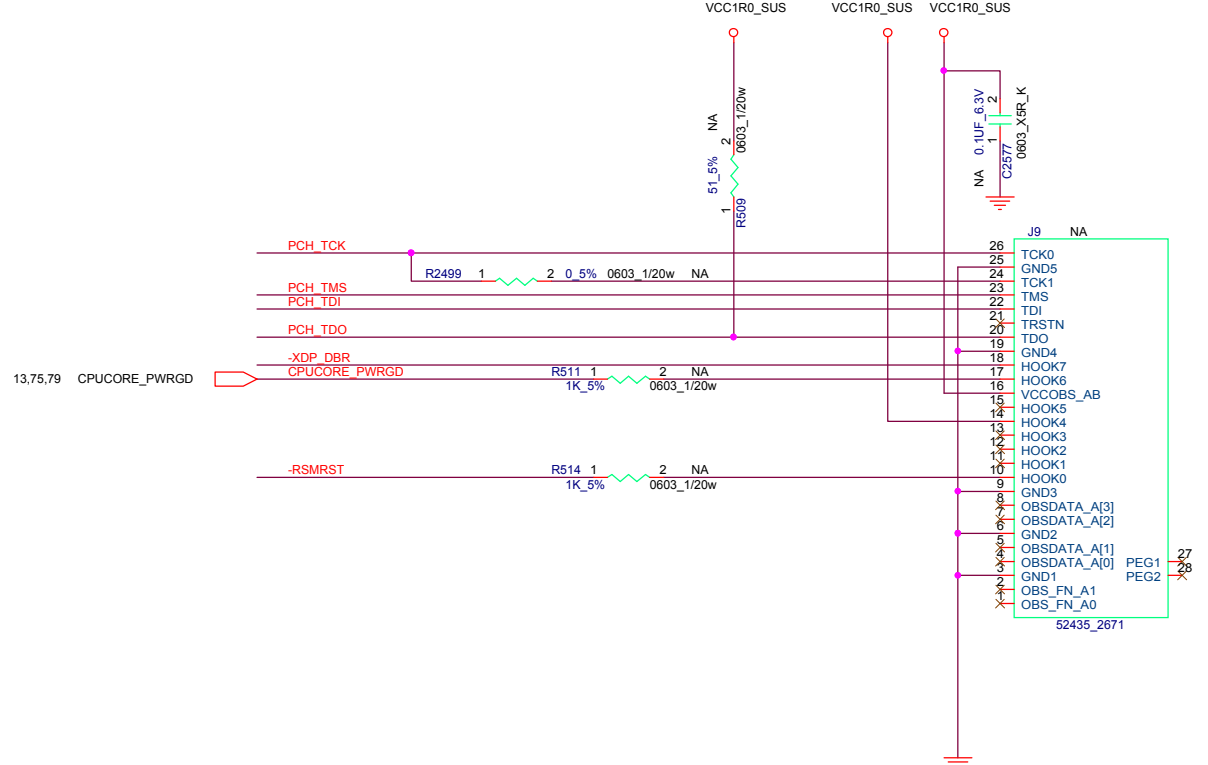
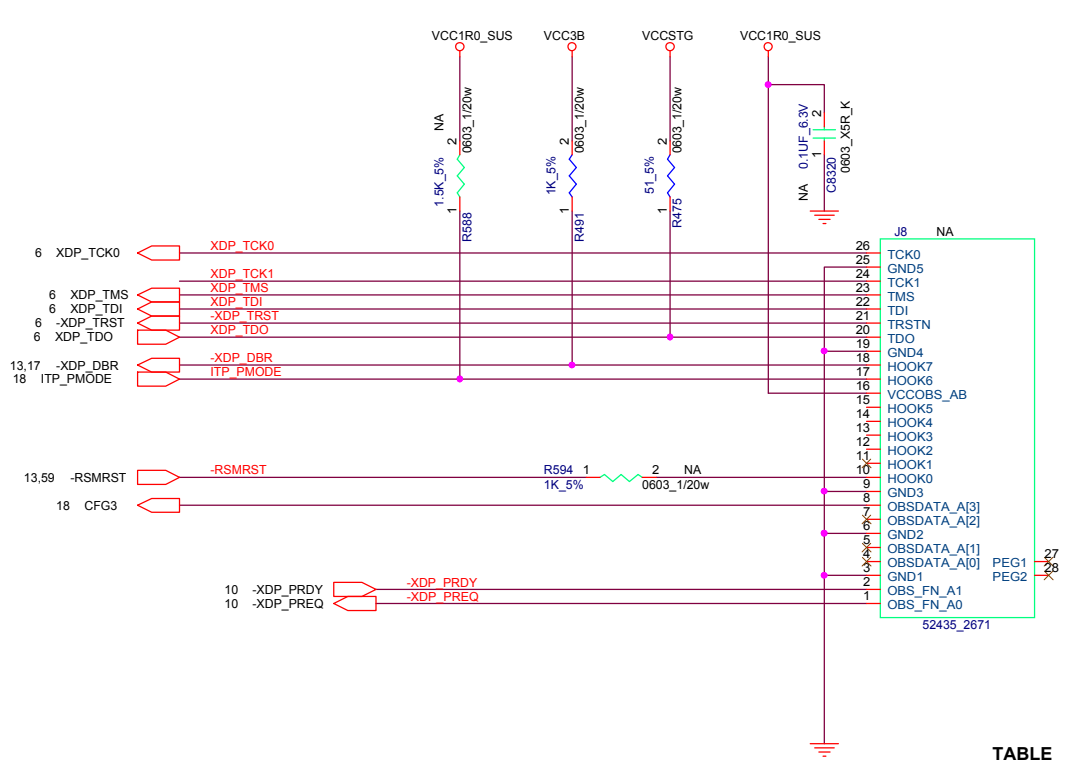
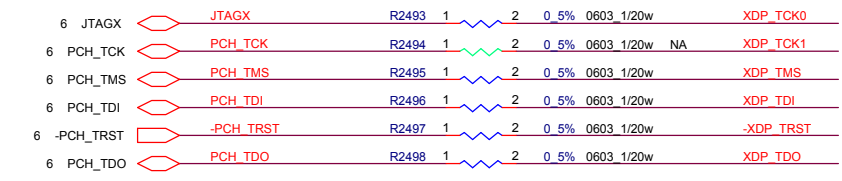
APS/PETS Interface



<p>CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall</p>
<p>CFG3 : MSR Privacy Bit Feature 1 : MSR (C80h) bit[0] setting 0 : MSR (C80h) bit[0] overridden</p>
<p>CFG4 : eDP Enable 1 : Disabled 0 : Enabled</p>
<p>CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled</p>



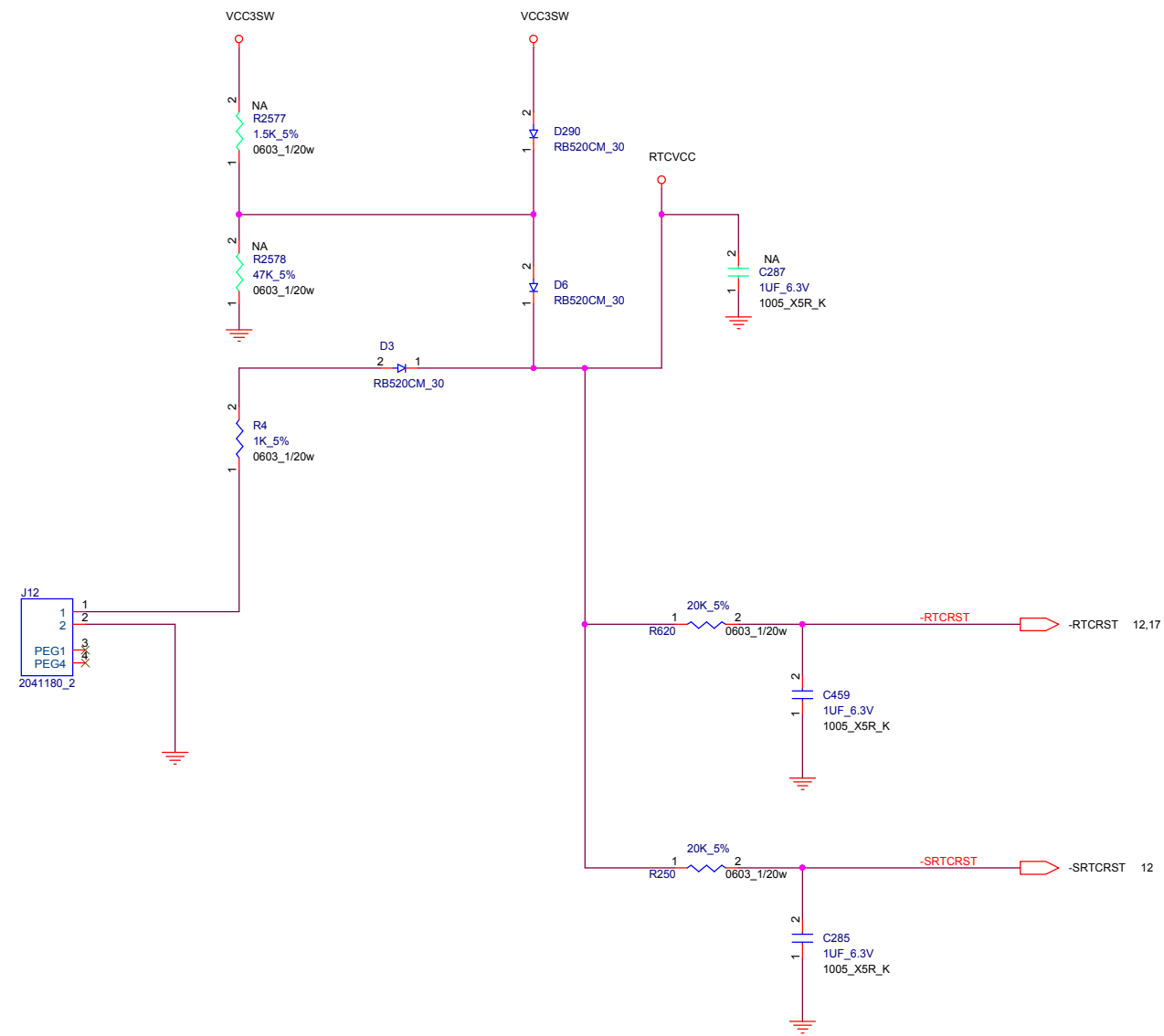
Project Name : THP1_SWG_SOVP		Title : CPU(16/16) : CFG/RESERVED	
Size : C	Document Number :		Rev : 8.04
Date: Tuesday, December 15, 2015		Sheet : 18 of 99	

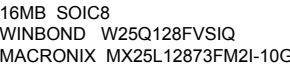


TABLE

Logic	Ref Des	Disabled	CPU XDP	ME XDP	Merged	DCI 2.0
Page 6	R2	ASM	ASM	ASM	ASM	ASM
	R471	ASM	ASM	ASM	NO_ASM	NO_ASM
	R541	NO_ASM	Don't Care	ASM	NO_ASM	NO_ASM
	R515	NO_ASM	Don't Care	ASM	NO_ASM	NO_ASM
	R530	NO_ASM	Don't Care	ASM	NO_ASM	NO_ASM
Page 7	R2559	NO_ASM	Don't Care	ASM	ASM	NO_ASM
Page 18	R1892	NO_ASM	ASM	Don't Care	ASM	NO_ASM
Page 19	J8	NO_ASM	ASM	Don't Care	ASM	NO_ASM
	C8320	NO_ASM	ASM	Don't Care	ASM	NO_ASM
	R475	NO_ASM	ASM	Don't Care	ASM	ASM
	R491	ASM	ASM	ASM	ASM	ASM
	R588	NO_ASM	ASM	Don't Care	ASM	NO_ASM
	R594	NO_ASM	ASM	Don't Care	ASM	NO_ASM
	J9	NO_ASM	Don't Care	ASM	NO_ASM	NO_ASM
	C2577	NO_ASM	Don't Care	ASM	NO_ASM	NO_ASM
	R2499	NO_ASM	Don't Care	NO_ASM	NO_ASM	NO_ASM
	R509	NO_ASM	Don't Care	ASM	NO_ASM	NO_ASM
	R511	NO_ASM	Don't Care	ASM	NO_ASM	NO_ASM
	R514	NO_ASM	Don't Care	ASM	NO_ASM	NO_ASM
	R2493	NO_ASM	NO_ASM	NO_ASM	ASM	ASM
	R2494	NO_ASM	NO_ASM	NO_ASM	ASM	NO_ASM
	R2495	NO_ASM	NO_ASM	NO_ASM	ASM	ASM
	R2496	NO_ASM	NO_ASM	NO_ASM	ASM	ASM
	R2497	NO_ASM	NO_ASM	NO_ASM	ASM	ASM
	R2498	NO_ASM	NO_ASM	NO_ASM	ASM	ASM
Page 21	R706	ASM	Don't Care	NO_ASM	NO_ASM	ASM

↑
LOGIC





1	VCC	D12.1	GND	GND	2
3	CS#	R322.2	R681.2	CLK	4
5	MISO	R694.2	R674.2	MOSI	6
7	(KEY)	N/A	N/A	(RESET)	8

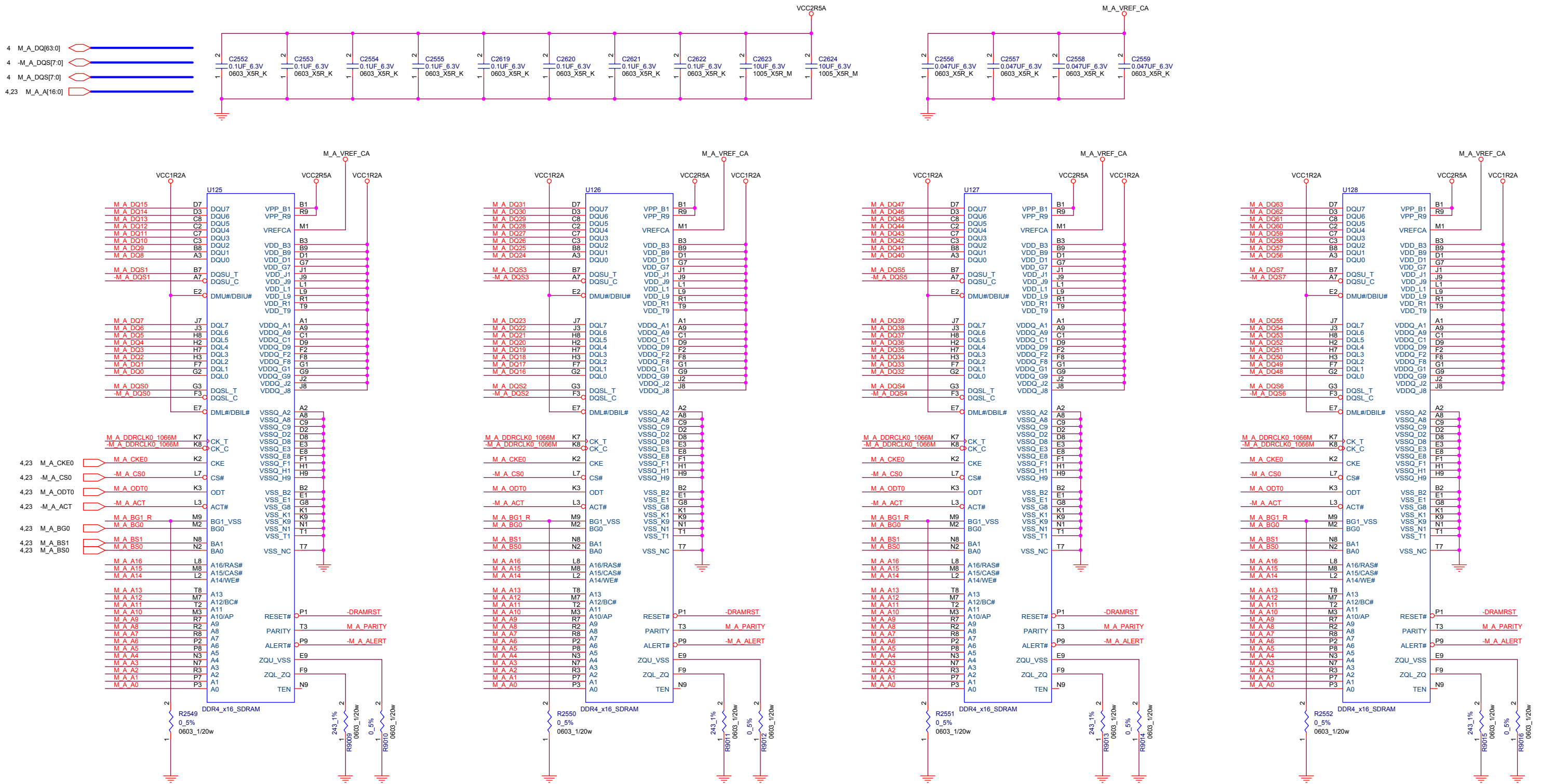
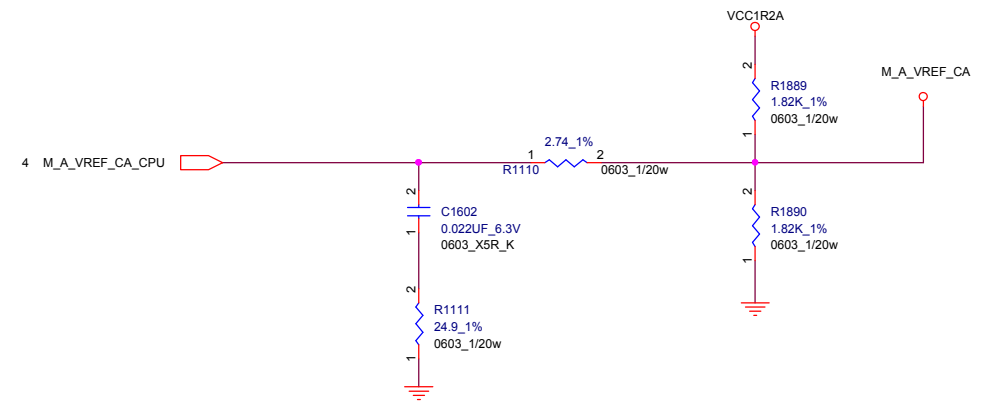
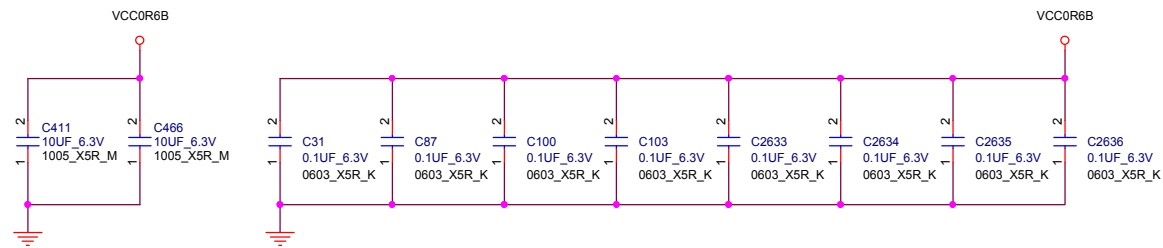
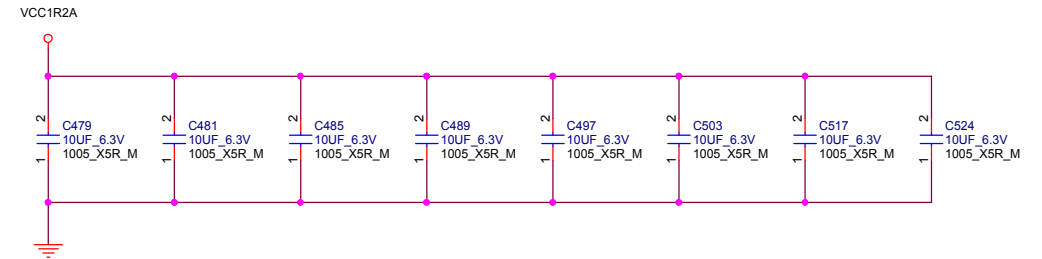
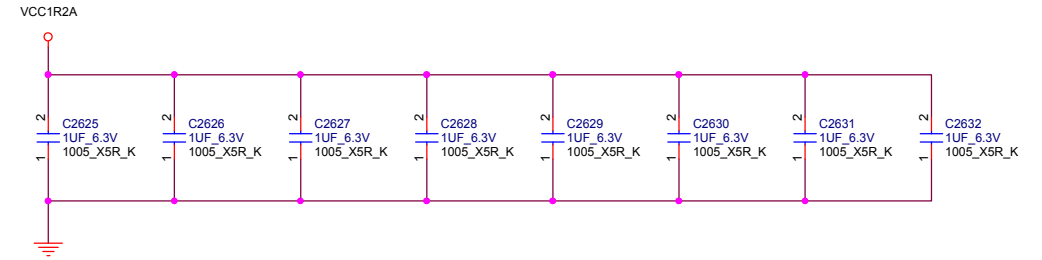
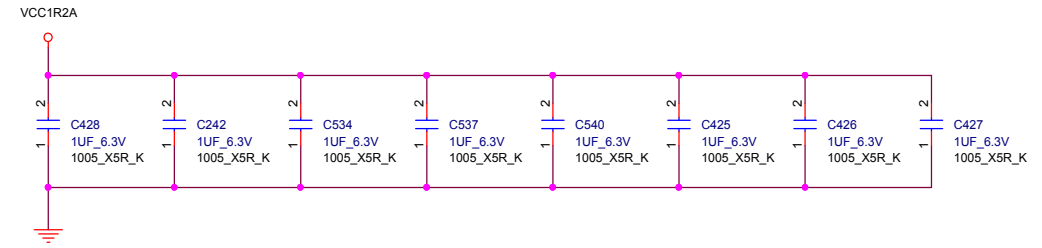
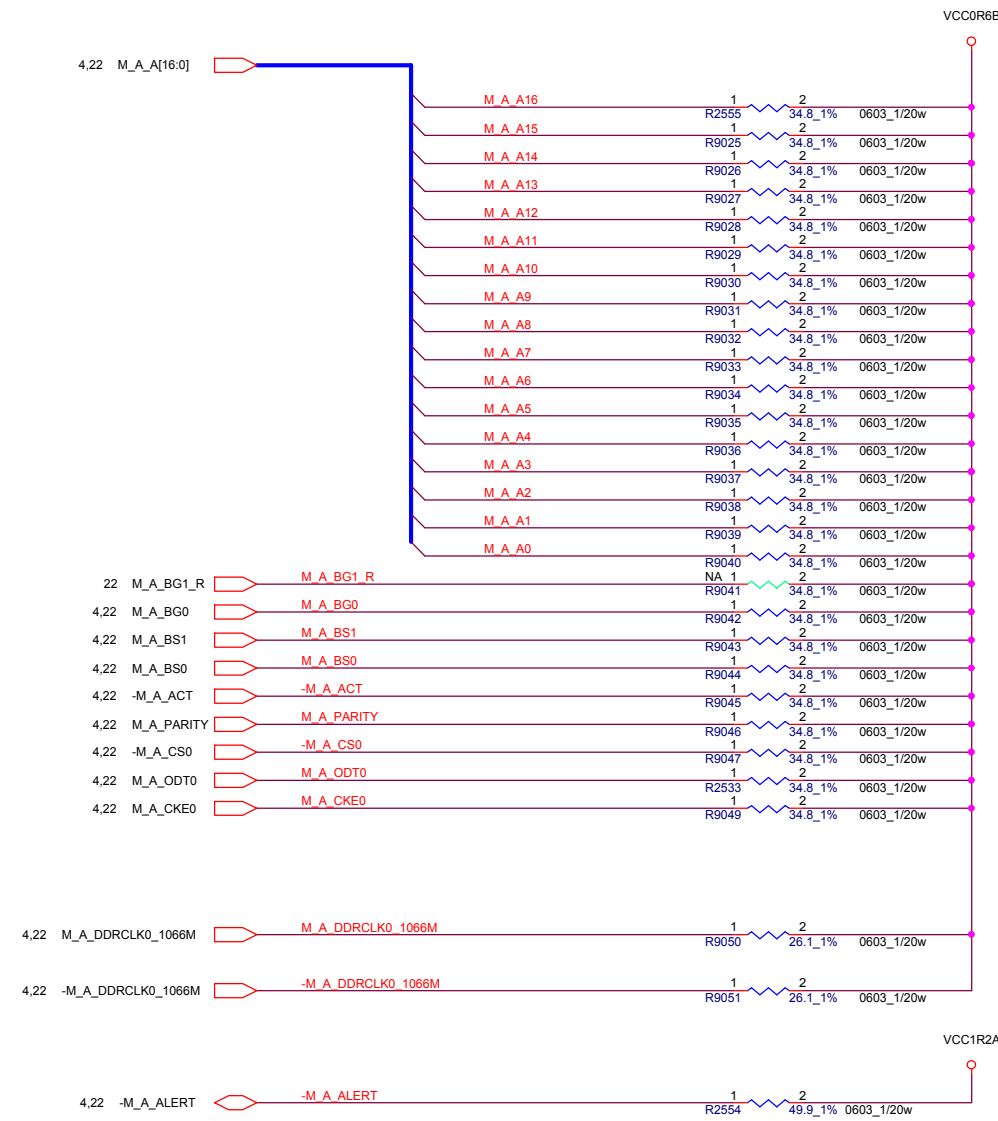


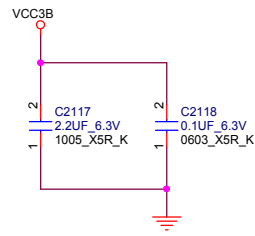
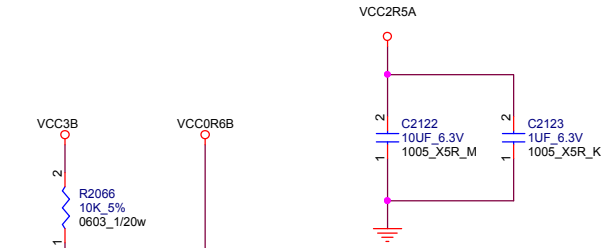
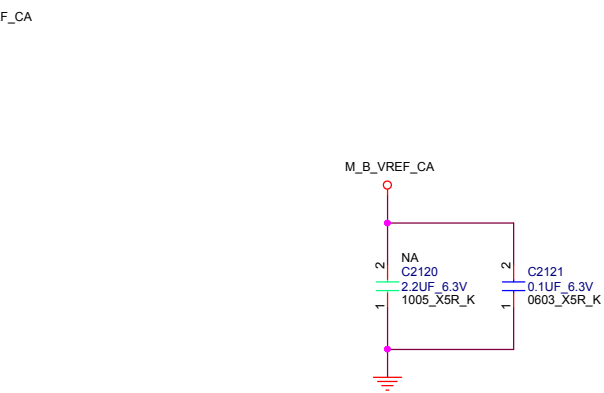
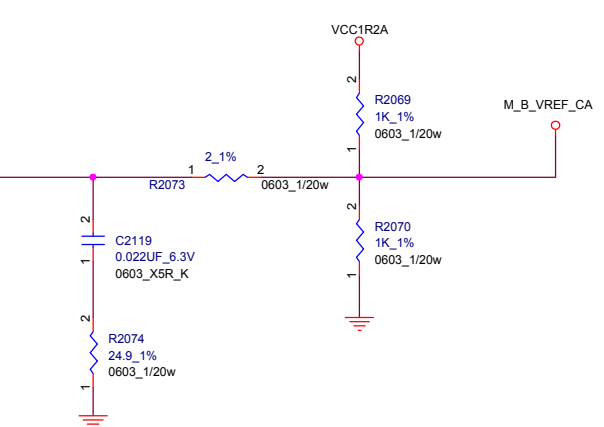
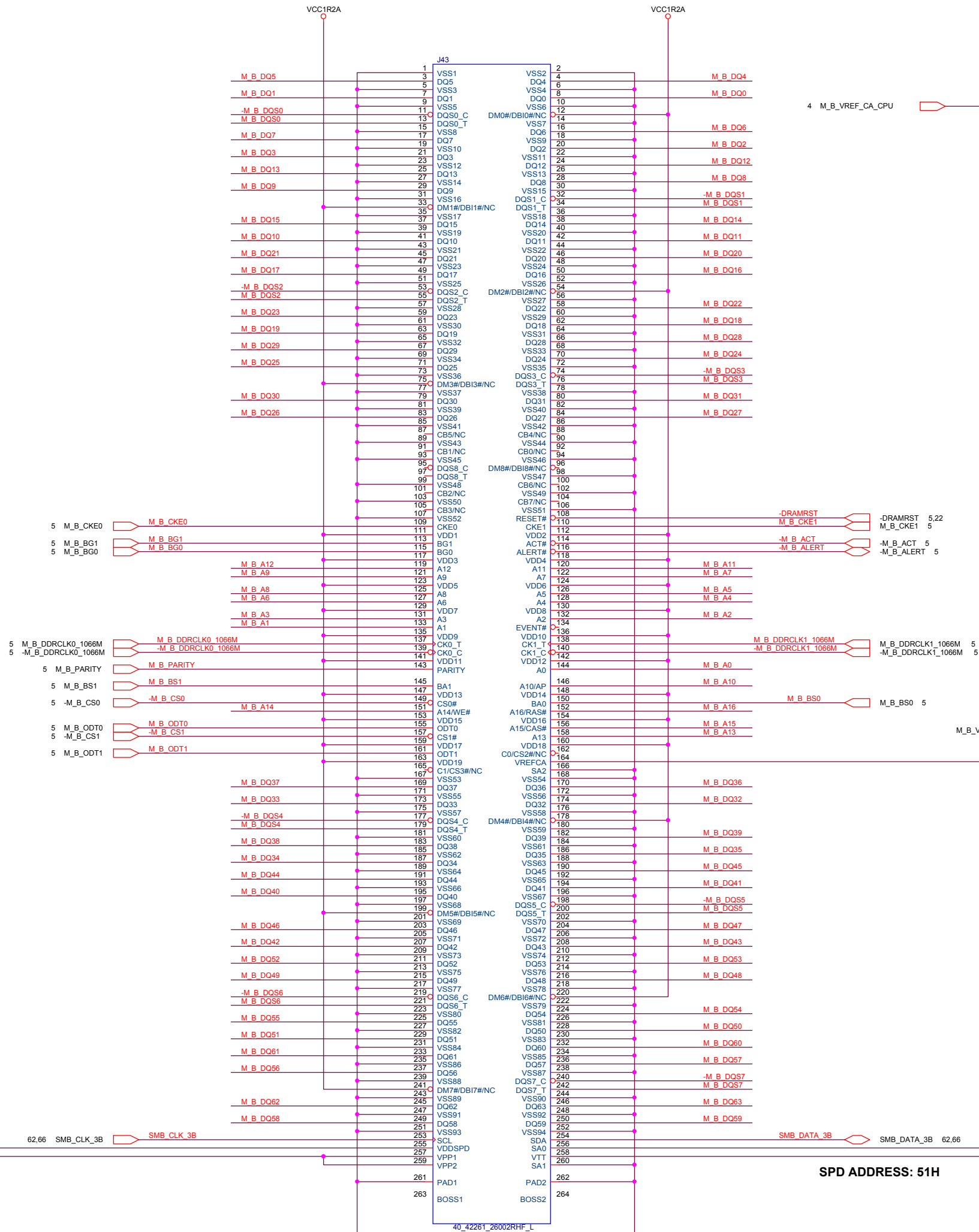
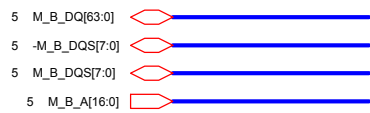
TABLE:

	SDP	DDP
R2549	ASM	NA
R2550	ASM	NA
R2551	ASM	NA
R2552	ASM	NA
R2553	NA	ASM
R9041	NA	ASM
R9010	0_5%	243_1%
R9012	0_5%	243_1%
R9014	0_5%	243_1%
R9016	0_5%	243_1%

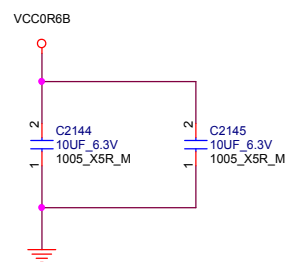
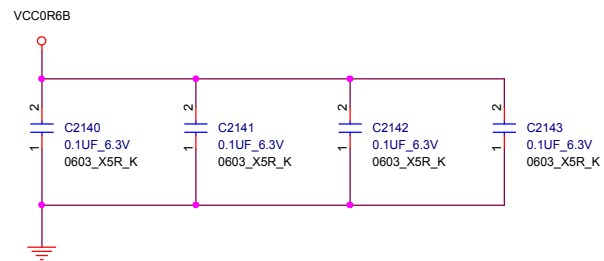
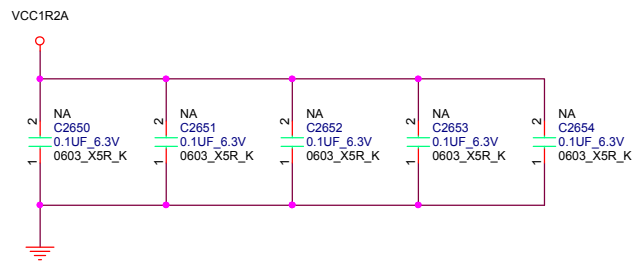
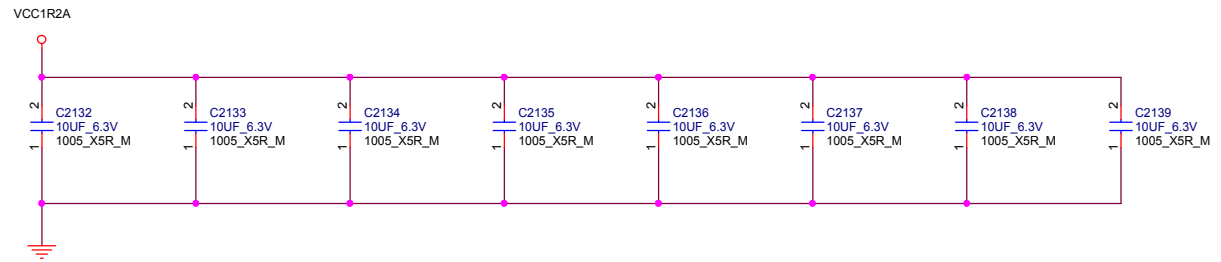
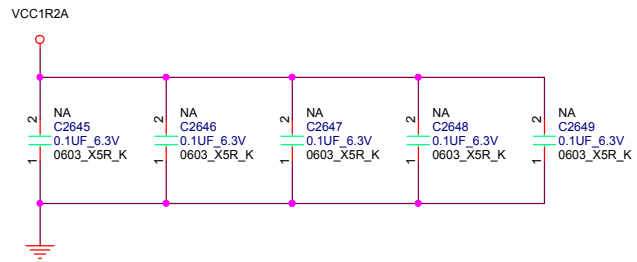
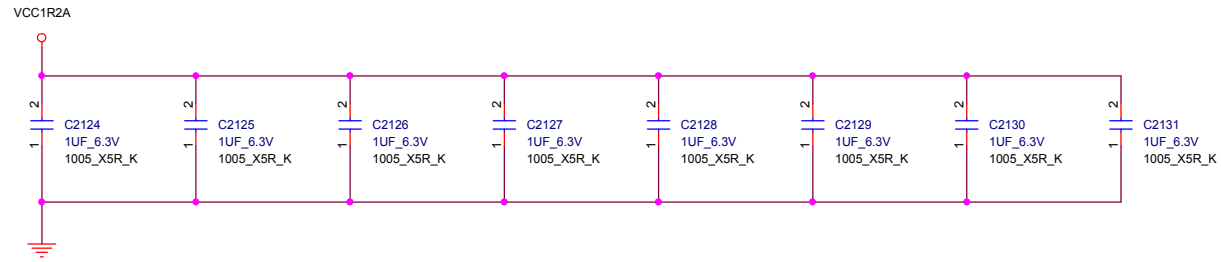
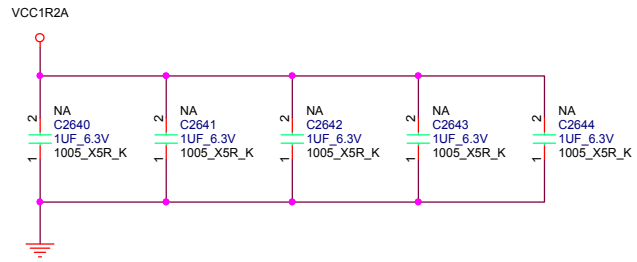
LOGIC

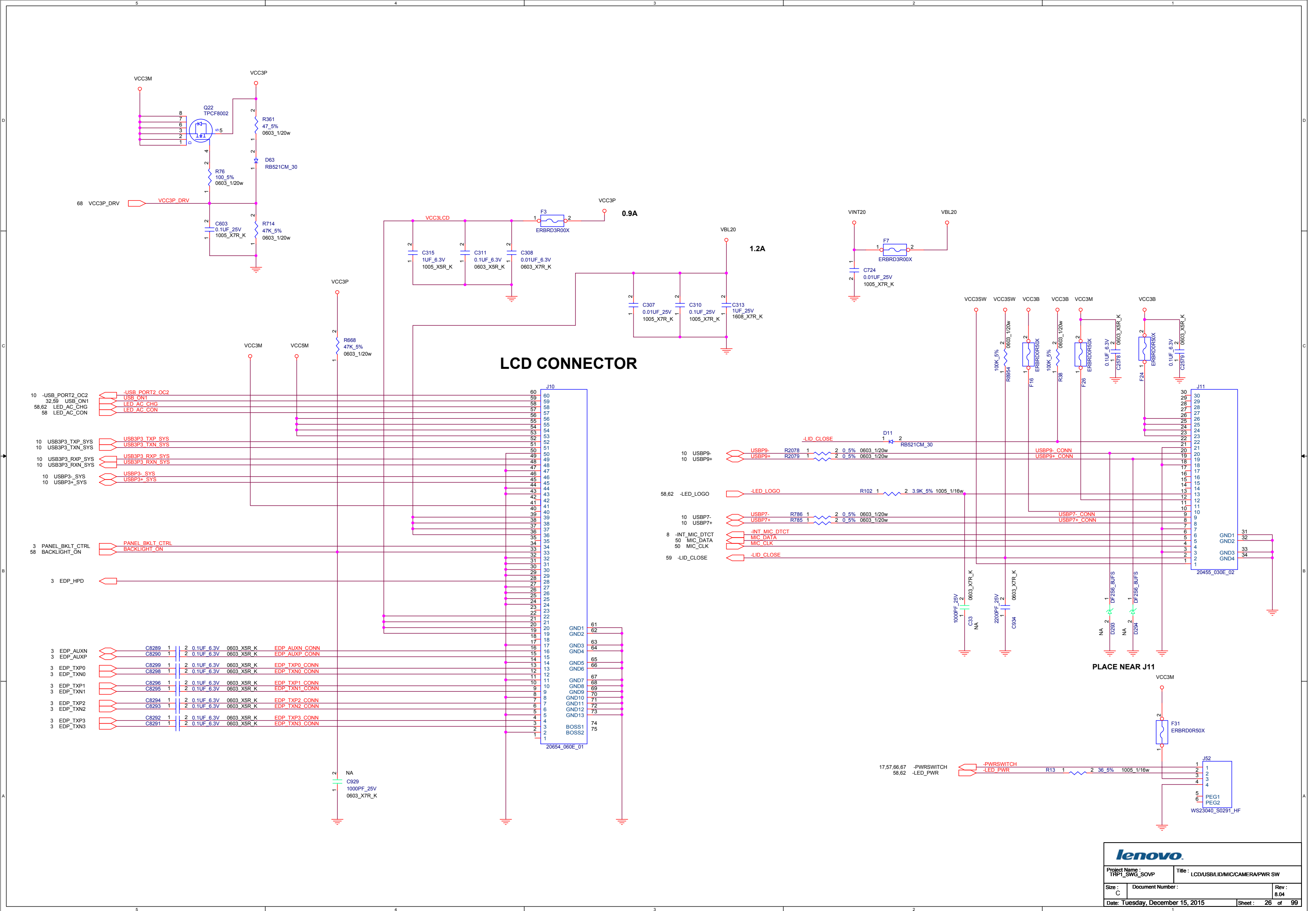






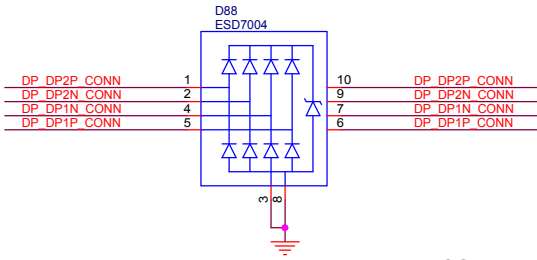
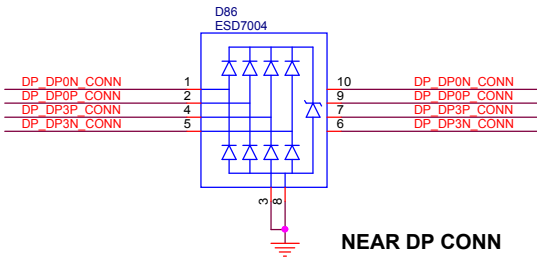
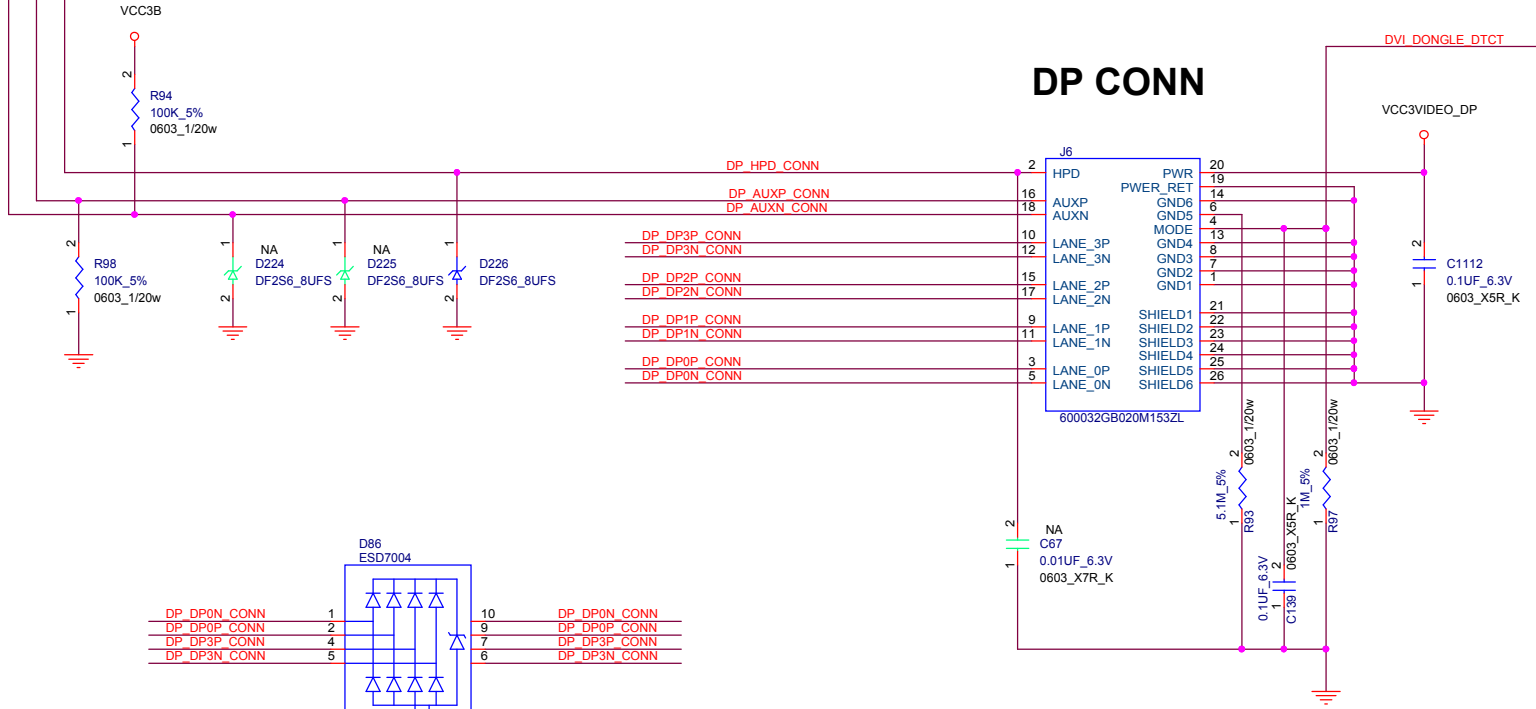
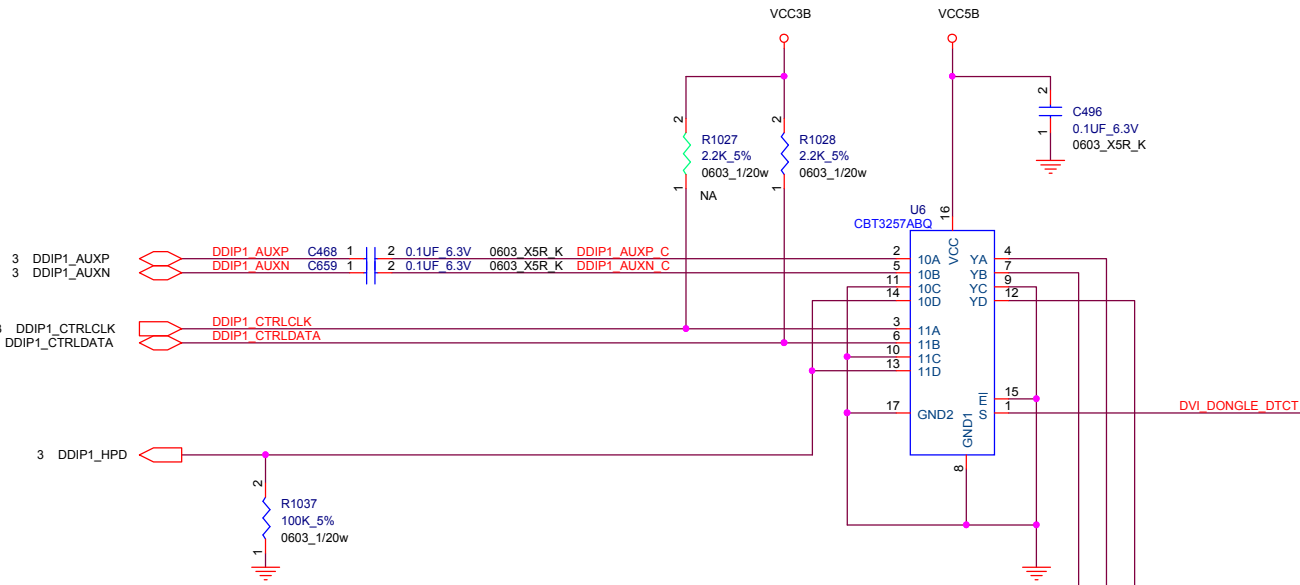
SPD ADDRESS: 51H



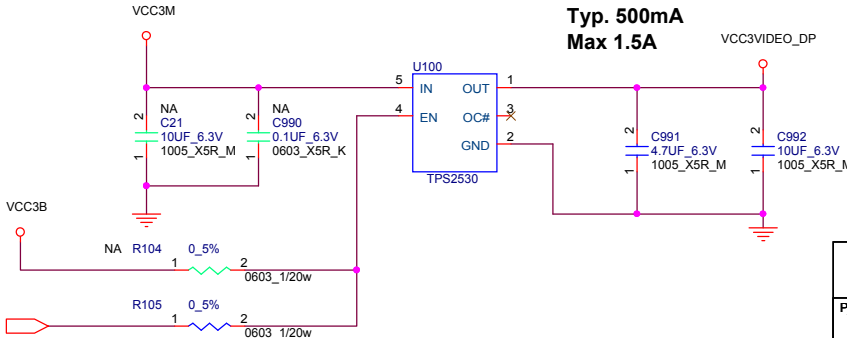


FOR SYSTEM DP NEAR DP CONN

3	DDIP1_3N		C339	1	2	0.1UF_6.3V	0603_X5R_K	DP_DP3N_CONN
3	DDIP1_3P		C323	1	2	0.1UF_6.3V	0603_X5R_K	DP_DP3P_CONN
3	DDIP1_2N		C312	1	2	0.1UF_6.3V	0603_X5R_K	DP_DP2N_CONN
3	DDIP1_2P		C317	1	2	0.1UF_6.3V	0603_X5R_K	DP_DP2P_CONN
3	DDIP1_1N		C277	1	2	0.1UF_6.3V	0603_X5R_K	DP_DP1N_CONN
3	DDIP1_1P		C276	1	2	0.1UF_6.3V	0603_X5R_K	DP_DP1P_CONN
3	DDIP1_0N		C218	1	2	0.1UF_6.3V	0603_X5R_K	DP_DP0N_CONN
3	DDIP1_0P		C226	1	2	0.1UF_6.3V	0603_X5R_K	DP_DP0P_CONN



NEAR DP CONN



NEAR DP CONN

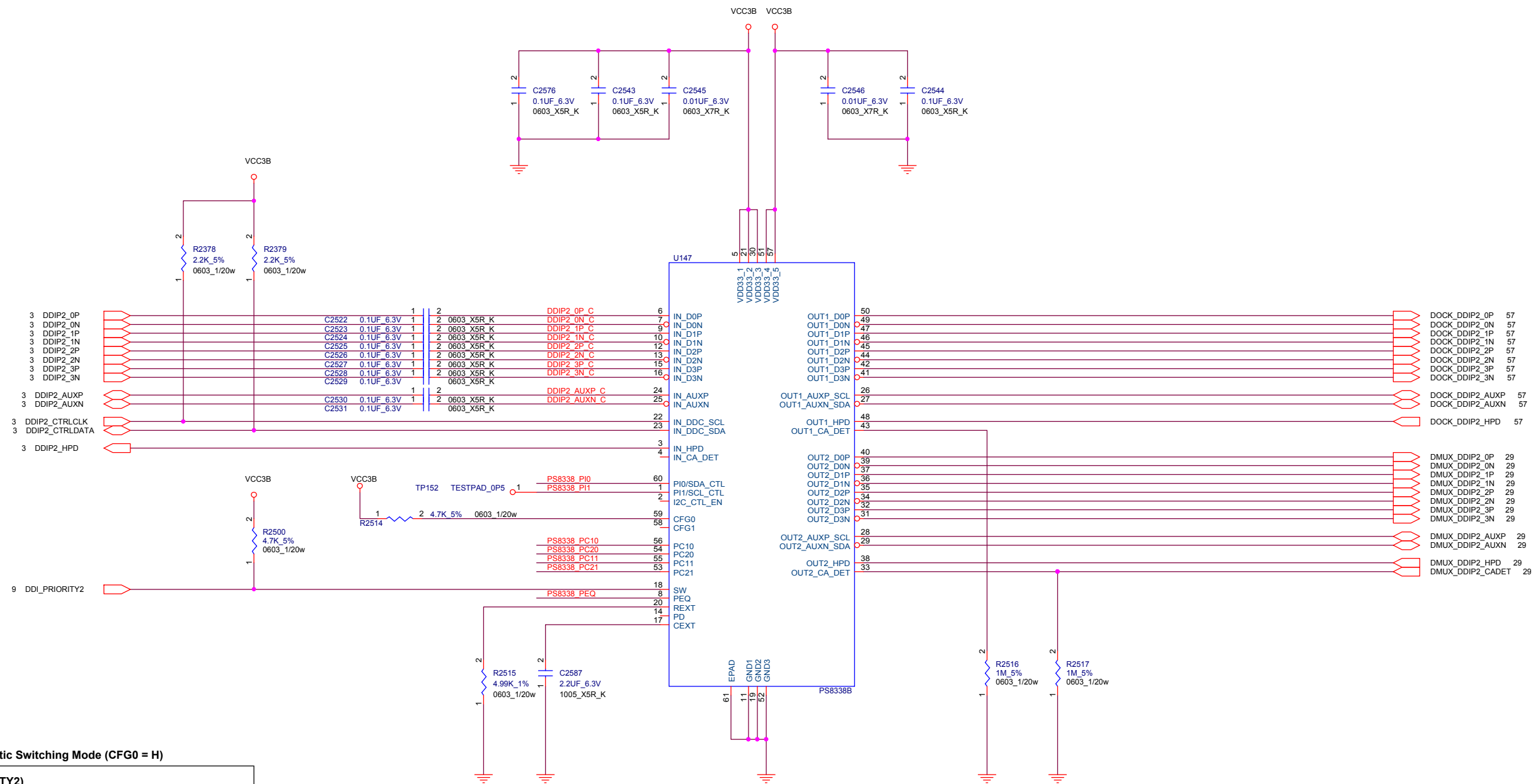
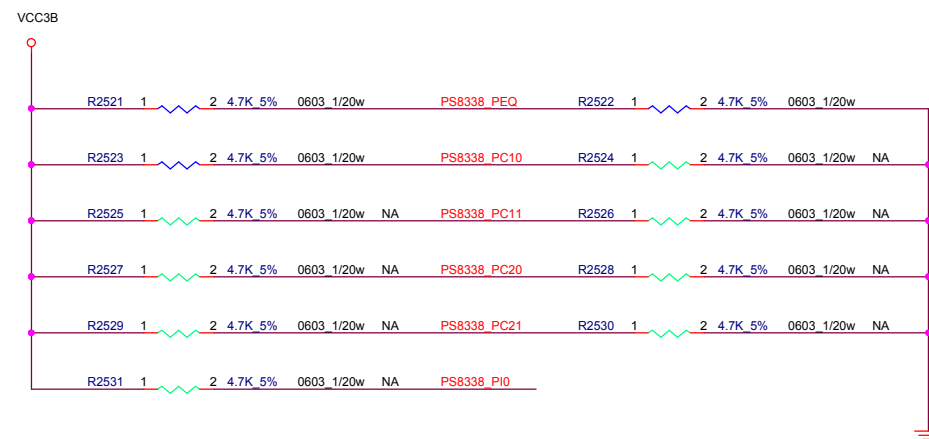
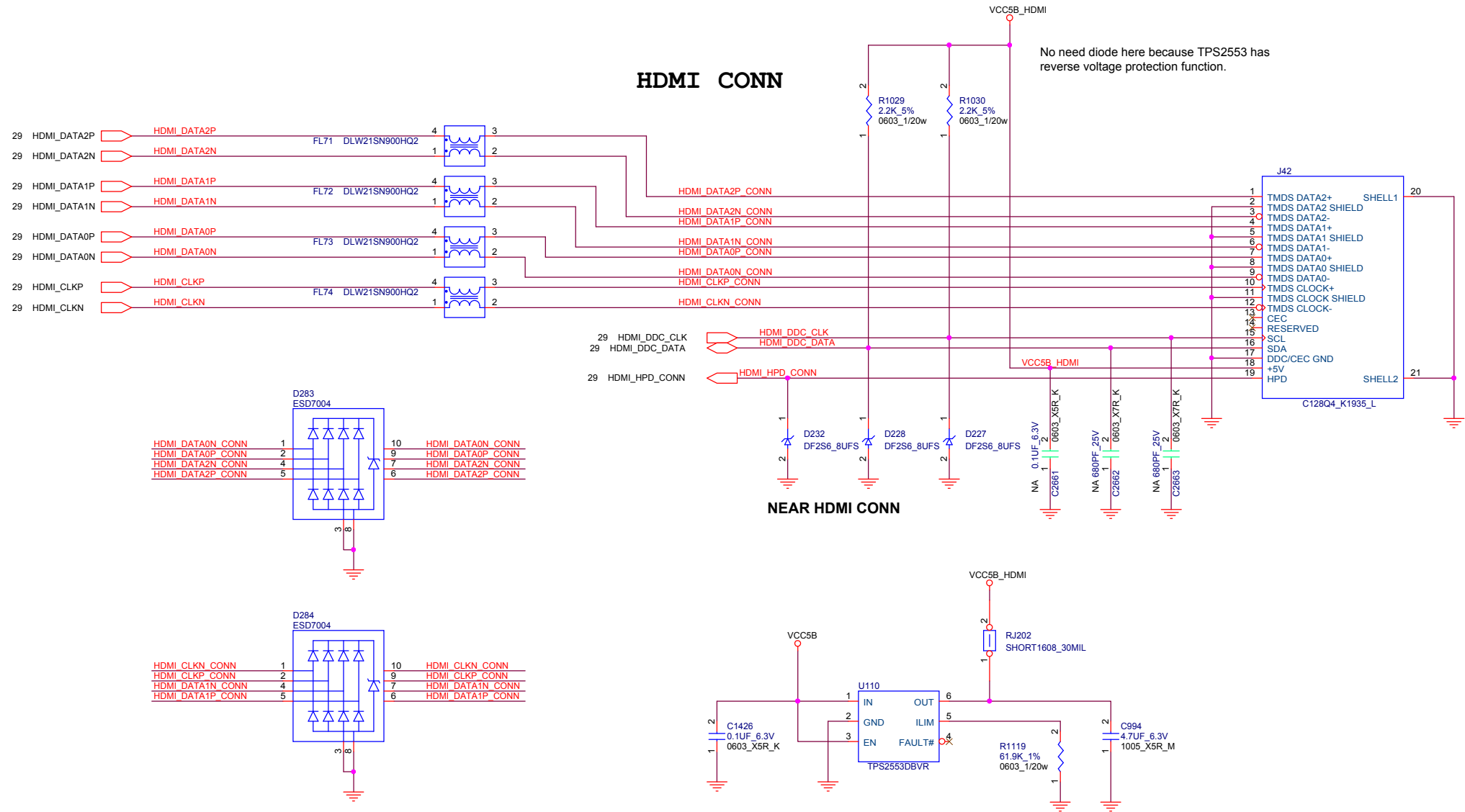


TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI_PRIORITY2)	
L	Port 1 has higher priority when both ports are plugged
H	Port 2 has higher priority when both ports are plugged

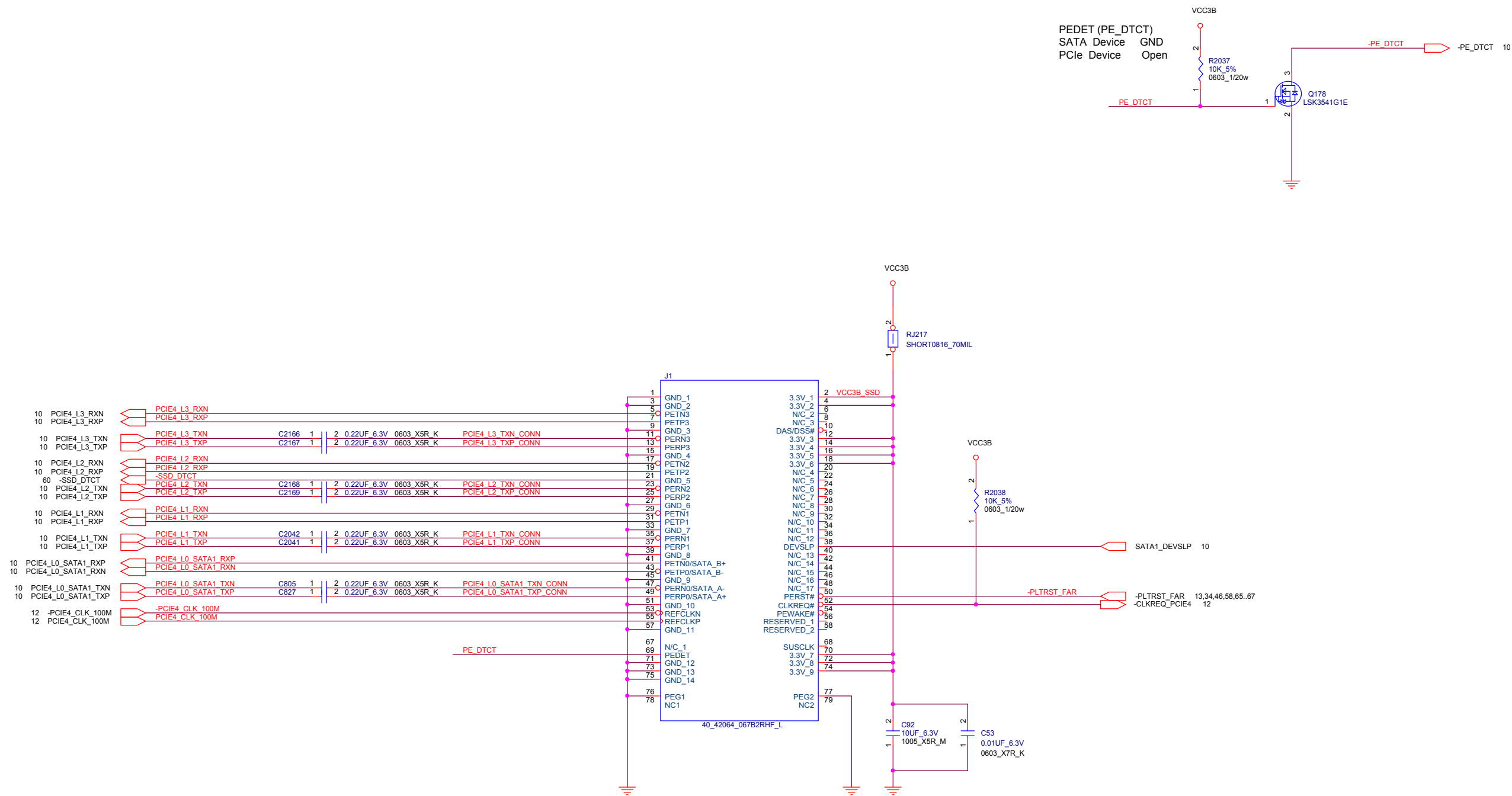




Project Name : THP1_SWG_SOVP Title : HDMI CONNECTOR

Size : C Document Number : Rev : 8.04

Date: Tuesday, December 15, 2015 Sheet: 30 of 99



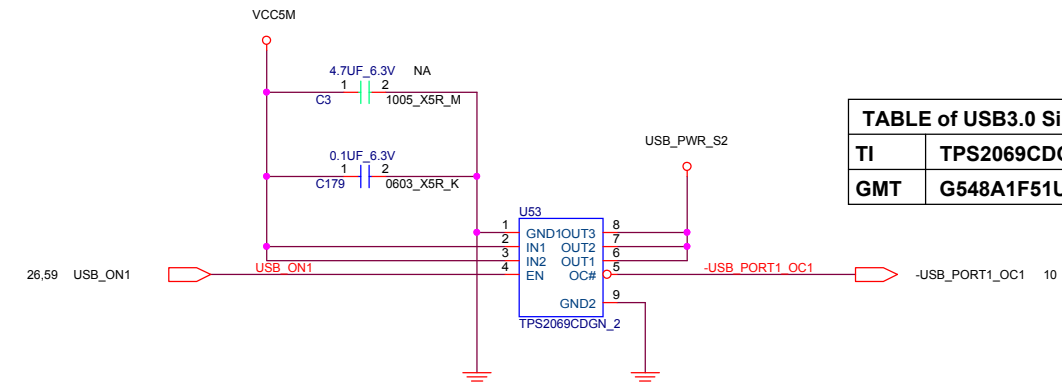
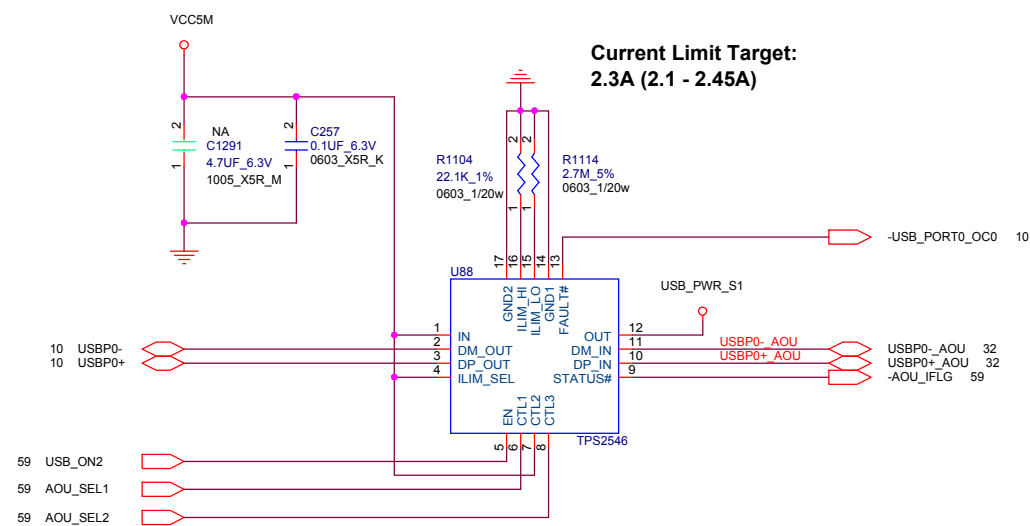
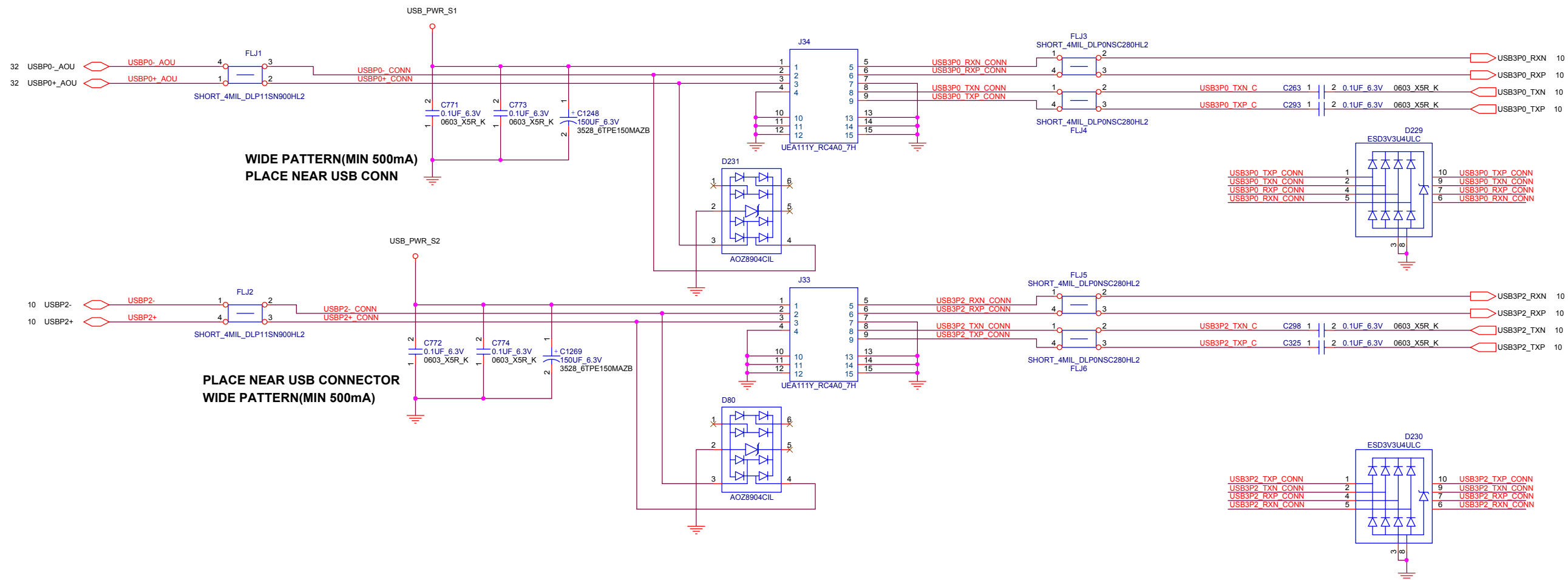
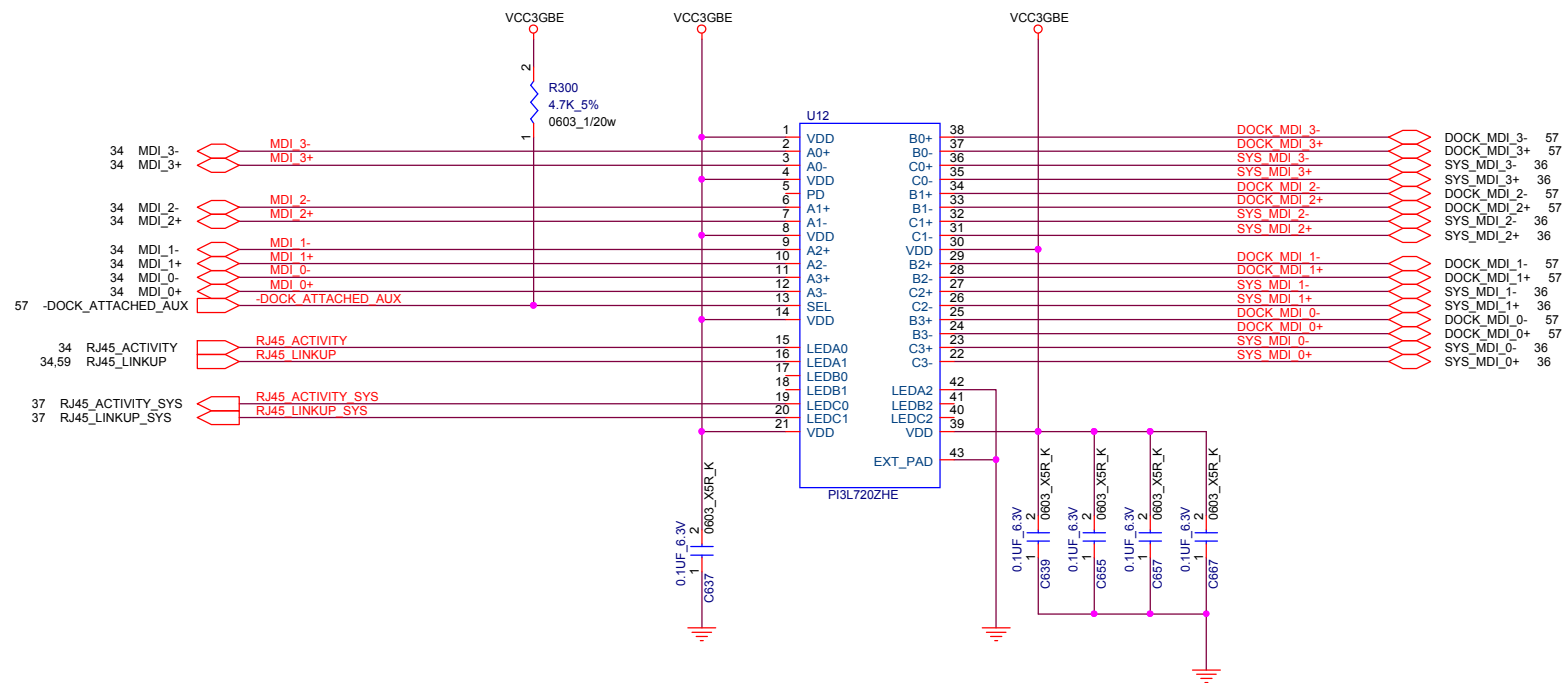
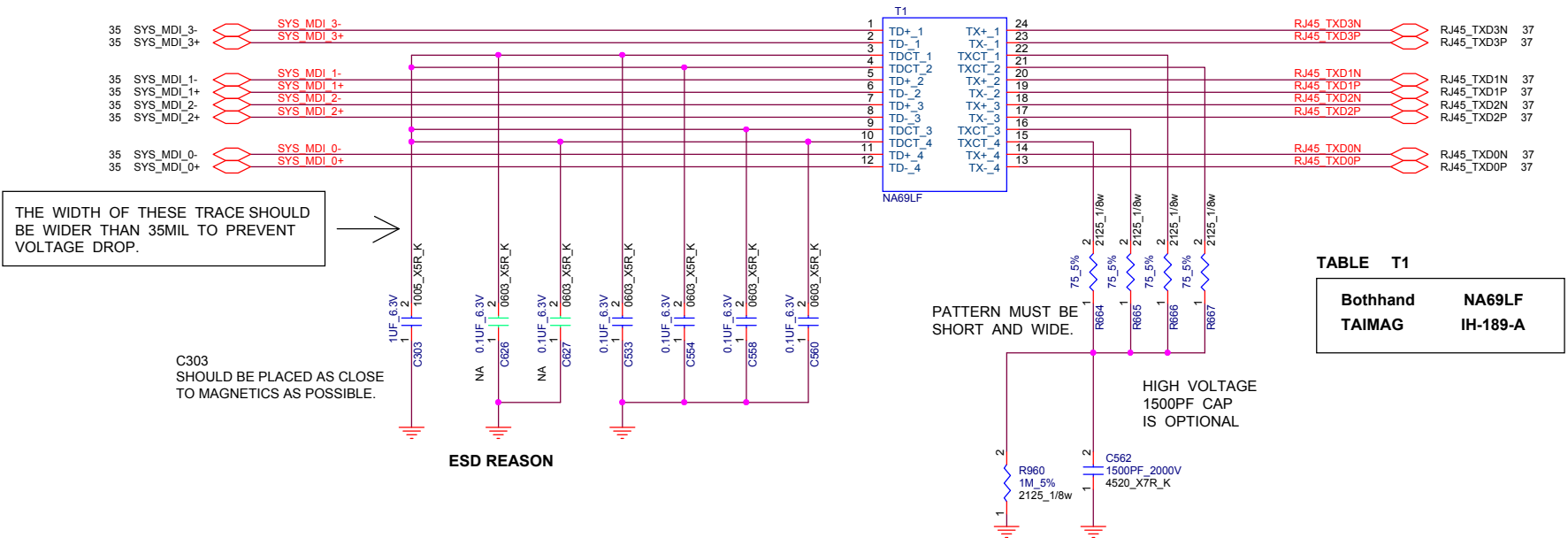


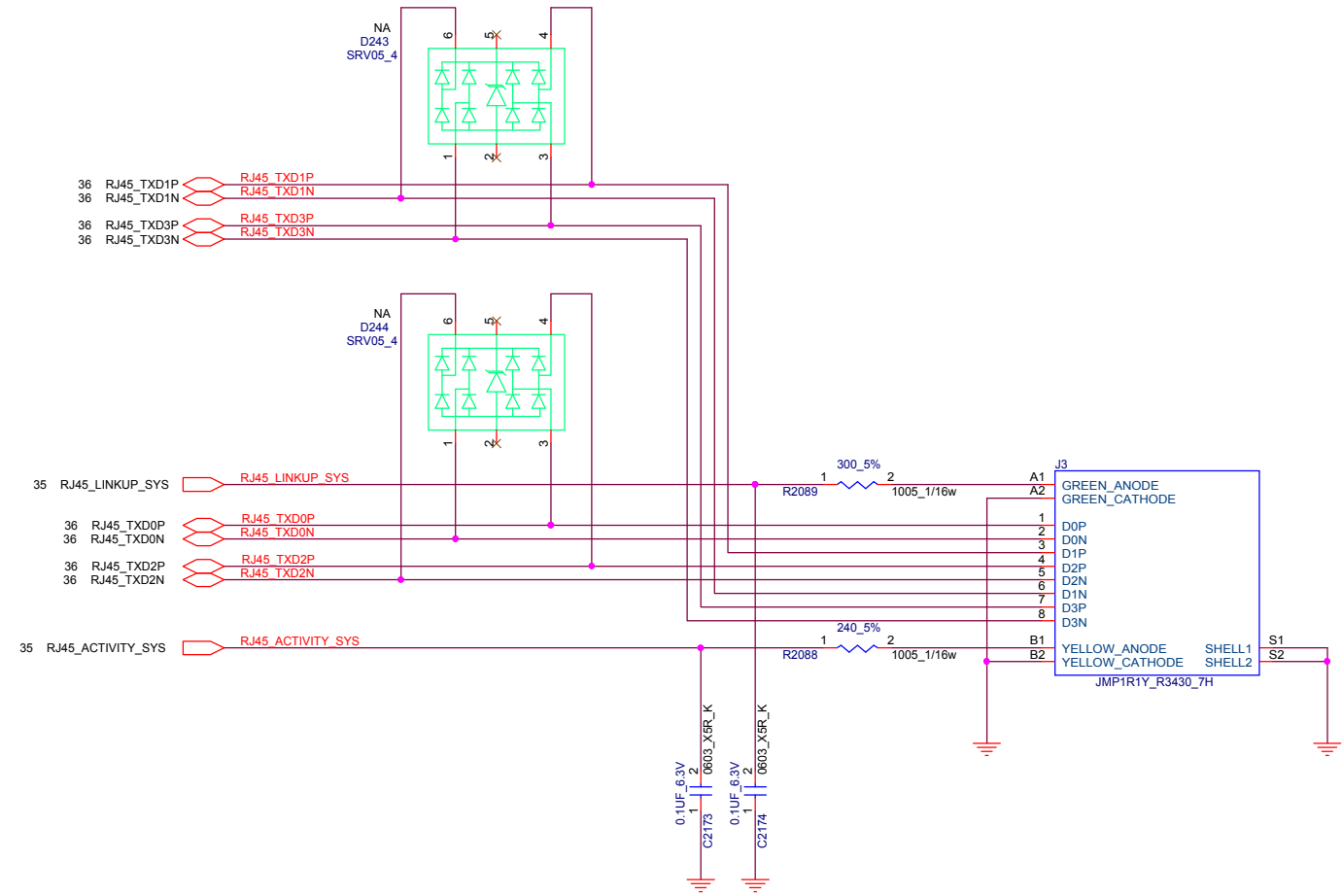
TABLE of USB3.0 Single	
TI	TPS2069CDGN-2
GMT	G548A1F51U

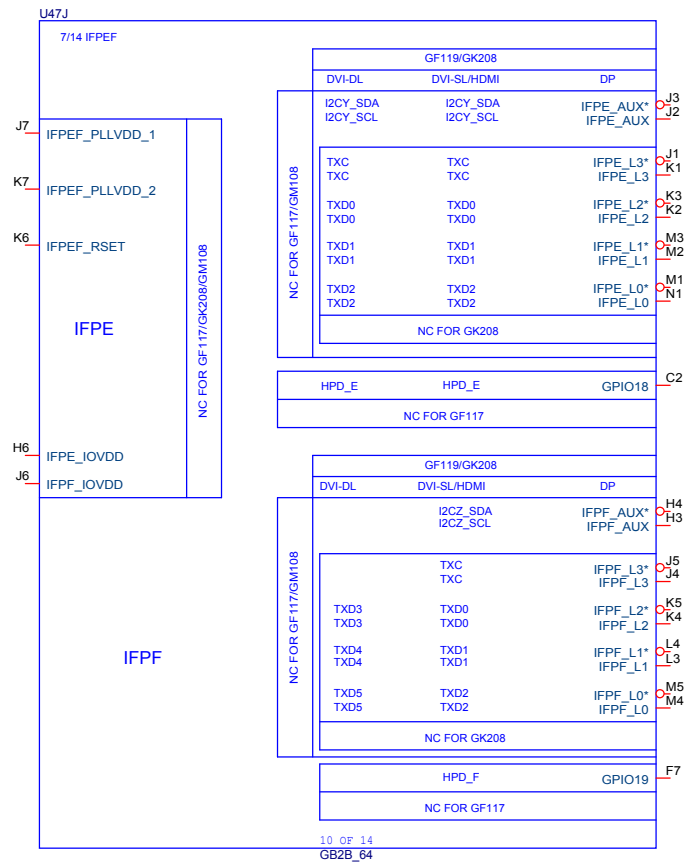
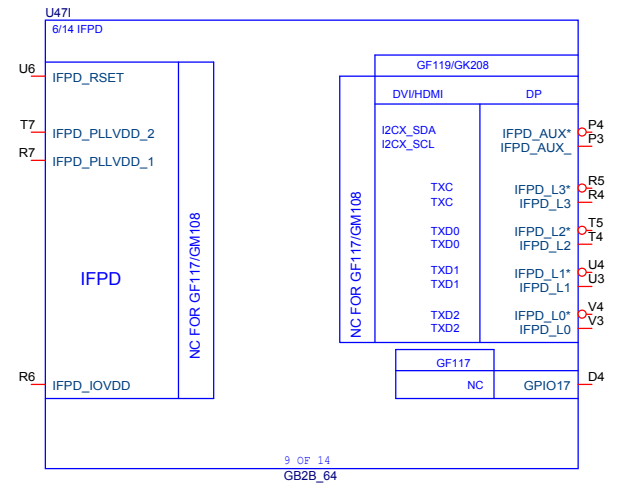
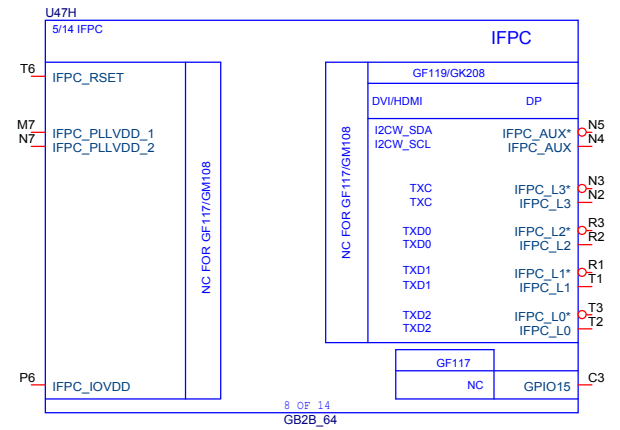
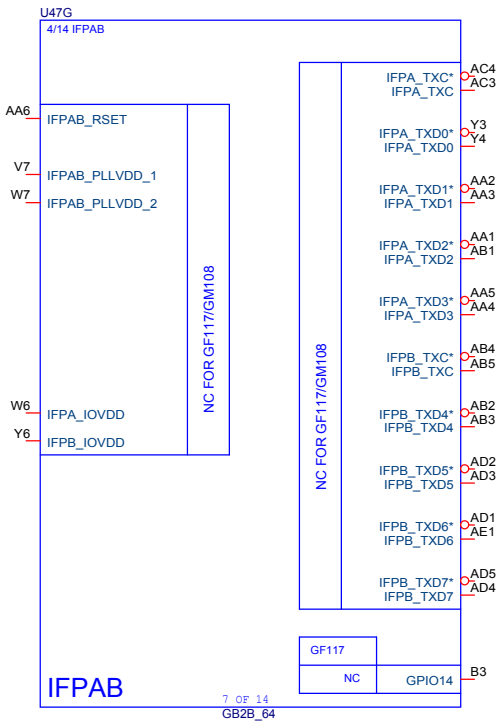


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44 FBA_D[63:0]

U47B

2/14 FBA

FBA_D0	E18	FBA_D0
FBA_D1	F18	FBA_D1
FBA_D2	E16	FBA_D2
FBA_D3	F17	FBA_D3
FBA_D4	D20	FBA_D4
FBA_D5	D21	FBA_D5
FBA_D6	F20	FBA_D6
FBA_D7	E21	FBA_D7
FBA_D8	E15	FBA_D8
FBA_D9	D15	FBA_D9
FBA_D10	F15	FBA_D10
FBA_D11	F13	FBA_D11
FBA_D12	C13	FBA_D12
FBA_D13	B13	FBA_D13
FBA_D14	E13	FBA_D14
FBA_D15	D13	FBA_D15
FBA_D16	B15	FBA_D16
FBA_D17	C16	FBA_D17
FBA_D18	A13	FBA_D18
FBA_D19	A15	FBA_D19
FBA_D20	B18	FBA_D20
FBA_D21	A18	FBA_D21
FBA_D22	A19	FBA_D22
FBA_D23	C19	FBA_D23
FBA_D24	B24	FBA_D24
FBA_D25	C23	FBA_D25
FBA_D26	A25	FBA_D26
FBA_D27	A24	FBA_D27
FBA_D28	A21	FBA_D28
FBA_D29	B21	FBA_D29
FBA_D30	C20	FBA_D30
FBA_D31	C21	FBA_D31
FBA_D32	R22	FBA_D32
FBA_D33	R24	FBA_D33
FBA_D34	T22	FBA_D34
FBA_D35	R23	FBA_D35
FBA_D36	N25	FBA_D36
FBA_D37	N26	FBA_D37
FBA_D38	N23	FBA_D38
FBA_D39	N24	FBA_D39
FBA_D40	V23	FBA_D40
FBA_D41	V22	FBA_D41
FBA_D42	T23	FBA_D42
FBA_D43	U22	FBA_D43
FBA_D44	T24	FBA_D44
FBA_D45	AA24	FBA_D45
FBA_D46	Y22	FBA_D46
FBA_D47	AA23	FBA_D47
FBA_D48	AD27	FBA_D48
FBA_D49	AB25	FBA_D49
FBA_D50	AD26	FBA_D50
FBA_D51	AC25	FBA_D51
FBA_D52	AA27	FBA_D52
FBA_D53	AA26	FBA_D53
FBA_D54	W26	FBA_D54
FBA_D55	Y25	FBA_D55
FBA_D56	R26	FBA_D56
FBA_D57	T25	FBA_D57
FBA_D58	N27	FBA_D58
FBA_D59	R27	FBA_D59
FBA_D60	V26	FBA_D60
FBA_D61	V27	FBA_D61
FBA_D62	W27	FBA_D62
FBA_D63	W25	FBA_D63

NC	FB_CLAMP
GF119	

R2091
10K_5%
0603_1/20w

Frame Buffer Command Mapping

N16x DDR3 Mode D

FBA_CMD0	C27	-FBA_CS0	44
FBA_CMD1	C26		
FBA_CMD2	E24	FBA_ODT0	44
FBA_CMD3	F24	FBA_CKE0	44
FBA_CMD4	D27	FBA_A14	44
FBA_CMD5	D26	FBA_RST	44
FBA_CMD6	F25	FBA_A9	44
FBA_CMD7	F23	FBA_A7	44
FBA_CMD8	G22	FBA_A2	44
FBA_CMD9	F27	FBA_A0	44
FBA_CMD10	G23	FBA_A4	44
FBA_CMD11	G24	FBA_A1	44
FBA_CMD12	F27	FBA_BA0	44
FBA_CMD13	G27	-FBA_WE	44
FBA_CMD14	G26	FBA_A15	44
FBA_CMD15	G26	-FBA_CAS	44
FBA_CMD16	M24	-FBA_CS1	44
FBA_CMD17	M23		
FBA_CMD18	K24		
FBA_CMD19	K23	FBA_ODT1	44
FBA_CMD20	M27	FBA_CKE1	44
FBA_CMD21	M26	FBA_A13	44
FBA_CMD22	M25	FBA_A8	44
FBA_CMD23	K26	FBA_A6	44
FBA_CMD24	K22	FBA_A11	44
FBA_CMD25	J23	FBA_A5	44
FBA_CMD26	J25	FBA_A3	44
FBA_CMD27	J24	FBA_BA2	44
FBA_CMD28	K27	FBA_BA1	44
FBA_CMD29	K25	FBA_A12	44
FBA_CMD30	J27	FBA_A10	44
FBA_CMD31	J26	-FBA_RAS	44

44 FBA_DM0	D19	FBA_DQM0
44 FBA_DM1	D14	FBA_DQM1
44 FBA_DM2	C17	FBA_DQM2
44 FBA_DM3	C22	FBA_DQM3
44 FBA_DM4	P24	FBA_DQM4
44 FBA_DM5	W24	FBA_DQM5
44 FBA_DM6	AA25	FBA_DQM6
44 FBA_DM7	U25	FBA_DQM7
44 FBA_DQS0	E19	FBA_DQS_WP0
44 FBA_DQS1	C15	FBA_DQS_WP1
44 FBA_DQS2	B16	FBA_DQS_WP2
44 FBA_DQS3	R25	FBA_DQS_WP3
44 FBA_DQS4	W23	FBA_DQS_WP4
44 FBA_DQS5	AB26	FBA_DQS_WP5
44 FBA_DQS6	T26	FBA_DQS_WP6
44 FBA_DQS7		FBA_DQS_WP7
44 -FBA_DQS0	F19	FBA_DQS_RN0
44 -FBA_DQS1	C14	FBA_DQS_RN1
44 -FBA_DQS2	A16	FBA_DQS_RN2
44 -FBA_DQS3	A22	FBA_DQS_RN3
44 -FBA_DQS4	P25	FBA_DQS_RN4
44 -FBA_DQS5	W22	FBA_DQS_RN5
44 -FBA_DQS6	AB27	FBA_DQS_RN6
44 -FBA_DQS7	T27	FBA_DQS_RN7

GF117/GF119 GK208	
NC	FBA_CMD32
FBA_DEBUG0	FBA_CMD34
FBA_DEBUG1	FBA_CMD35

FBA_CLK0	D24	FBA_CLK0	44
FBA_CLK0*	D25	-FBA_CLK0	44
FBA_CLK1	N22	FBA_CLK1	44
FBA_CLK1*	M22	-FBA_CLK1	44

FBA_WCK01	D18		
FBA_WCK01*	C18		
FBA_WCK23	D17		
FBA_WCK23*	D16		
FBA_WCK45	T24		
FBA_WCK45*	U24		
FBA_WCK67	V24		
FBA_WCK67*	V25		

GF119	FB_PLLAVDD_1
NC	FB_PLLAVDD_2
FB_PLLAVDD	FB_DLLAVDD
GF117	

D23 FB_VREF_PROBE
2 OF 14
GB2B_64

30ohm@100MHz ESR=0.01

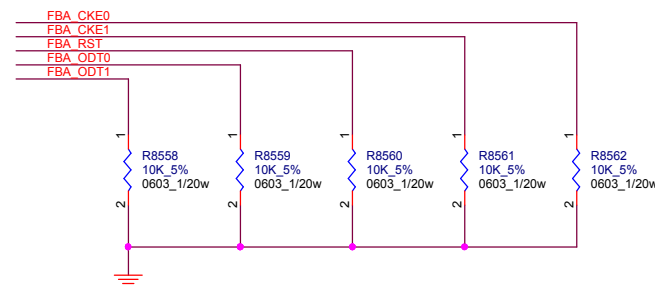
VCC1R0VIDEO

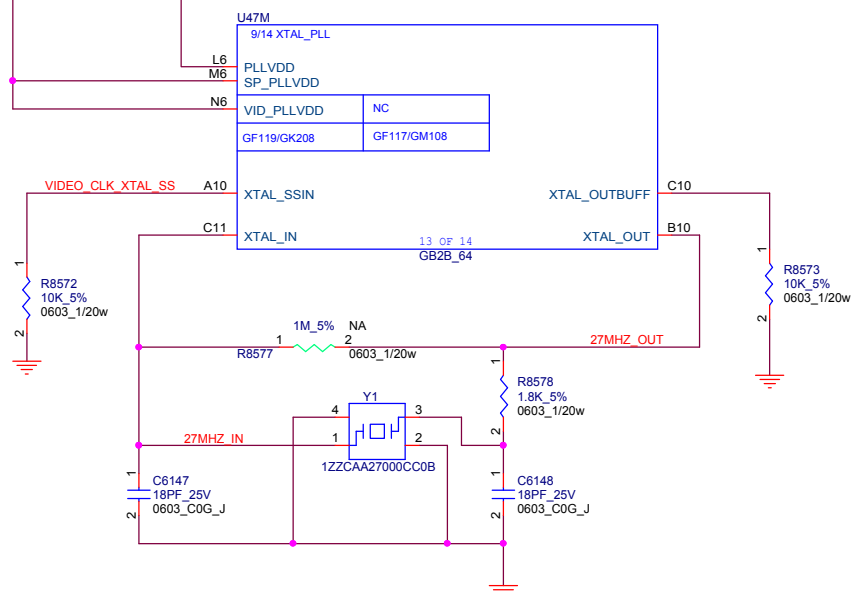
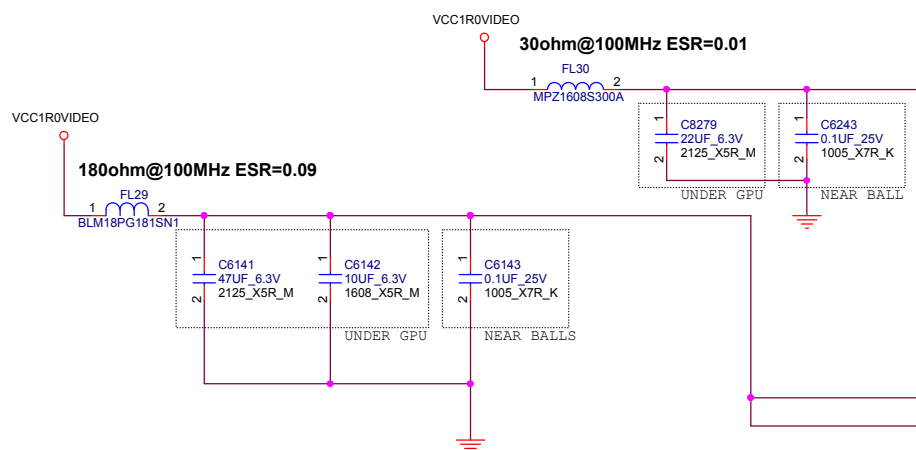
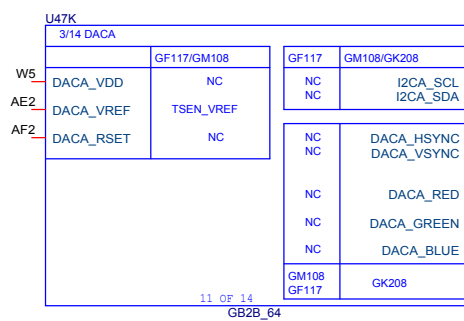
FL27
MPZ1608S300A

C6134
0.1UF_25V
1005_X7R_K

C6137
22UF_6.3V
2125_X5R_M

NEAR BALL





TXC 8Y27000002
Epson Q22FA1280025200

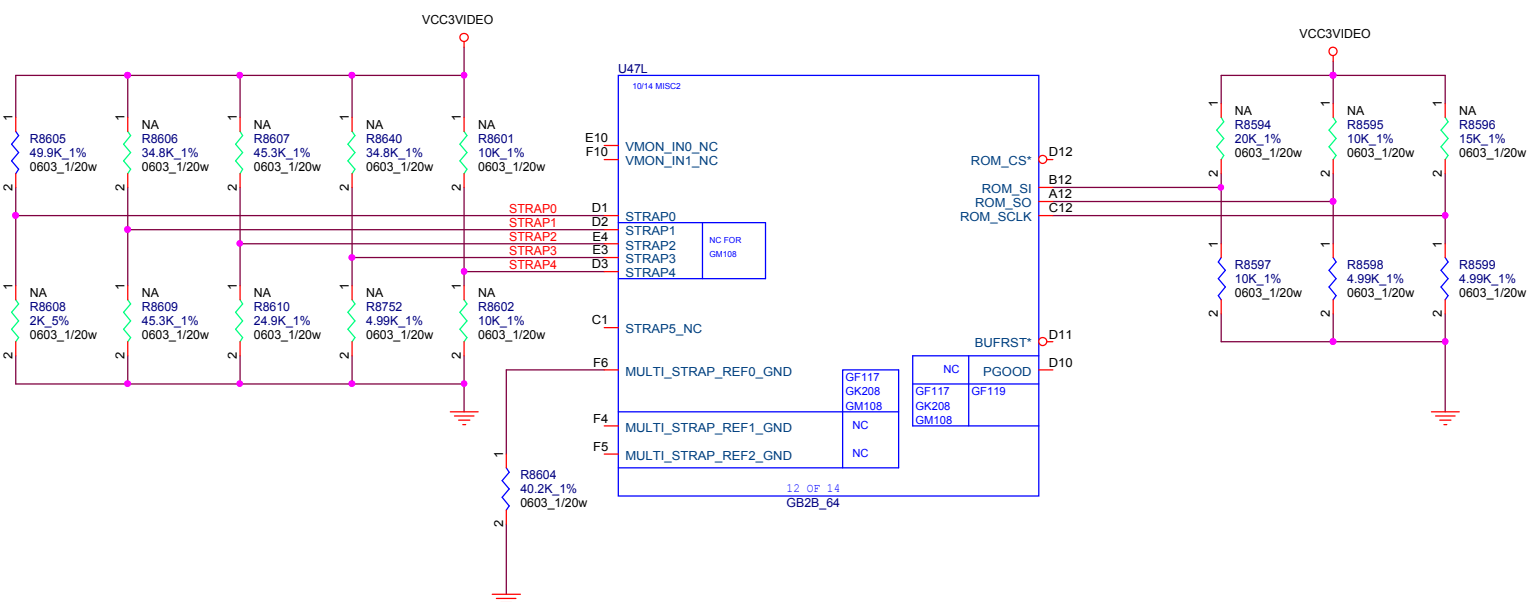
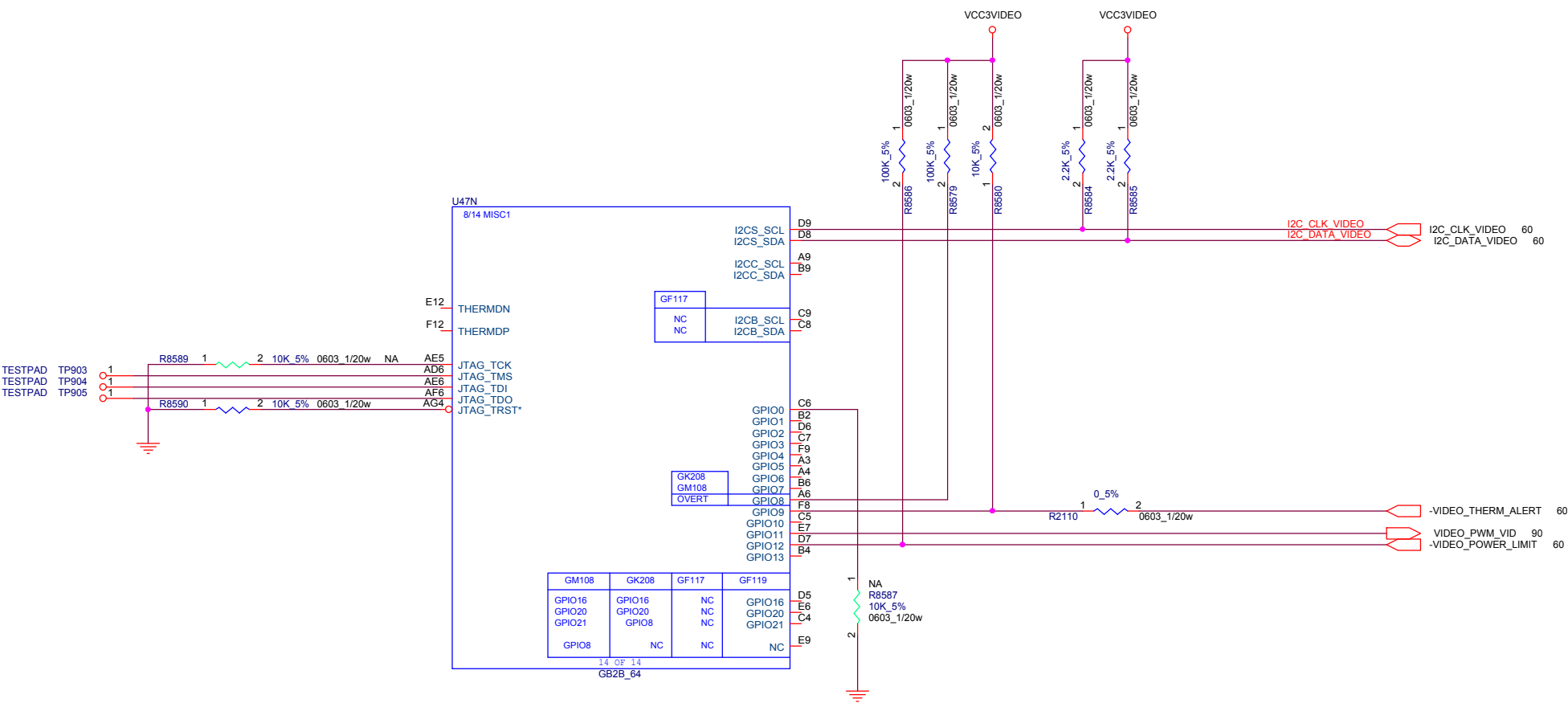
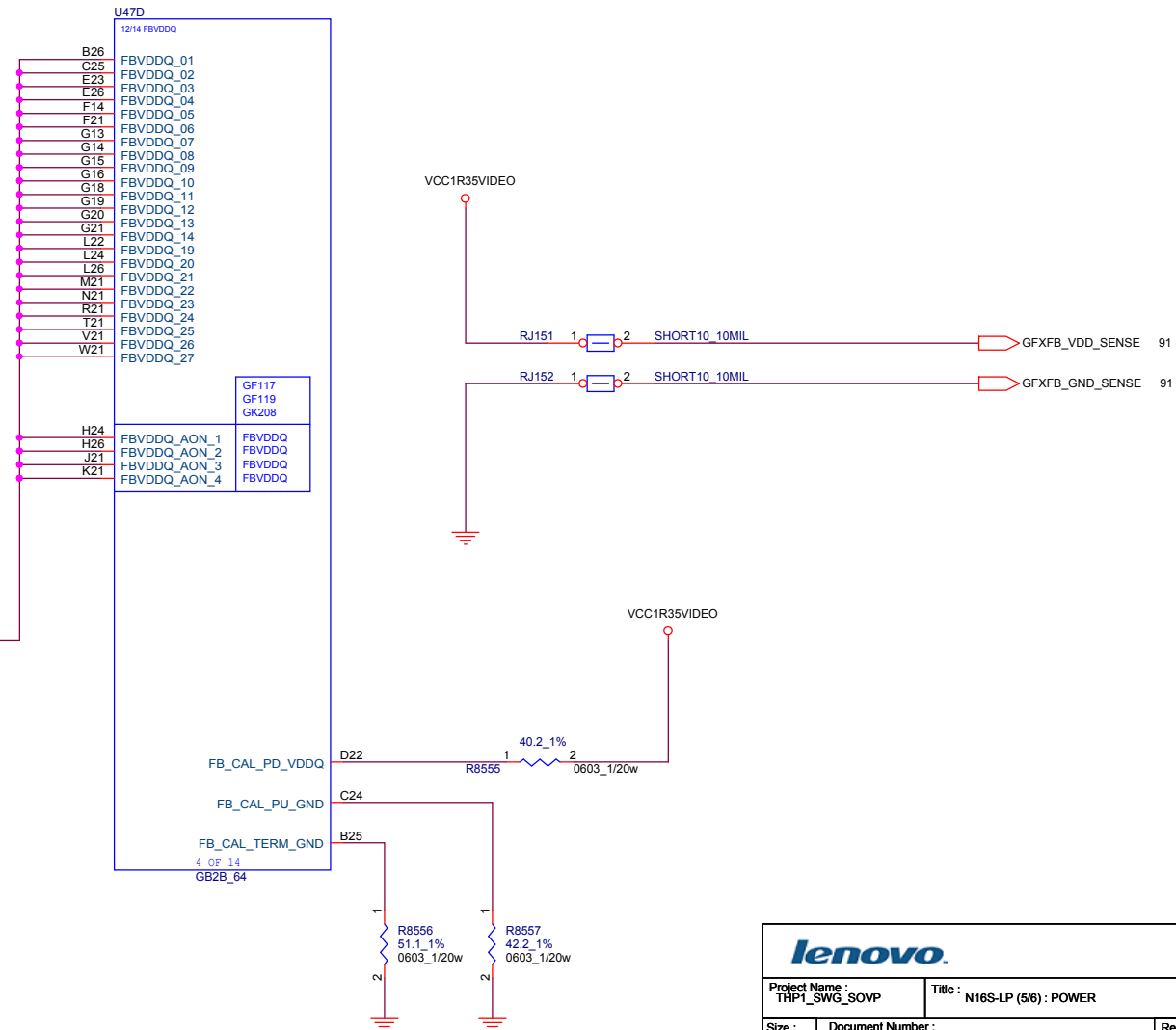
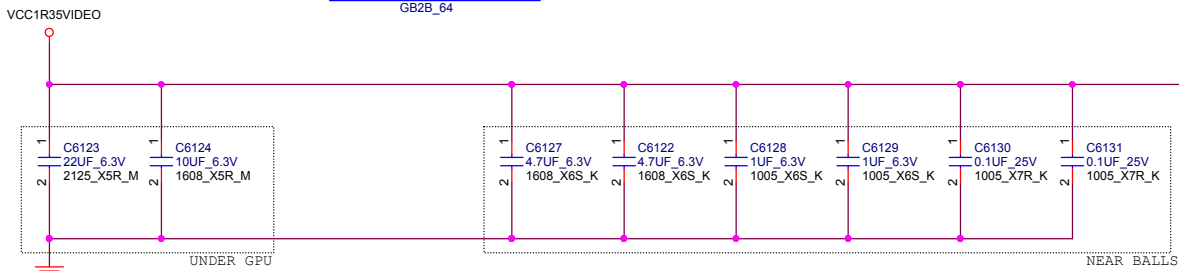
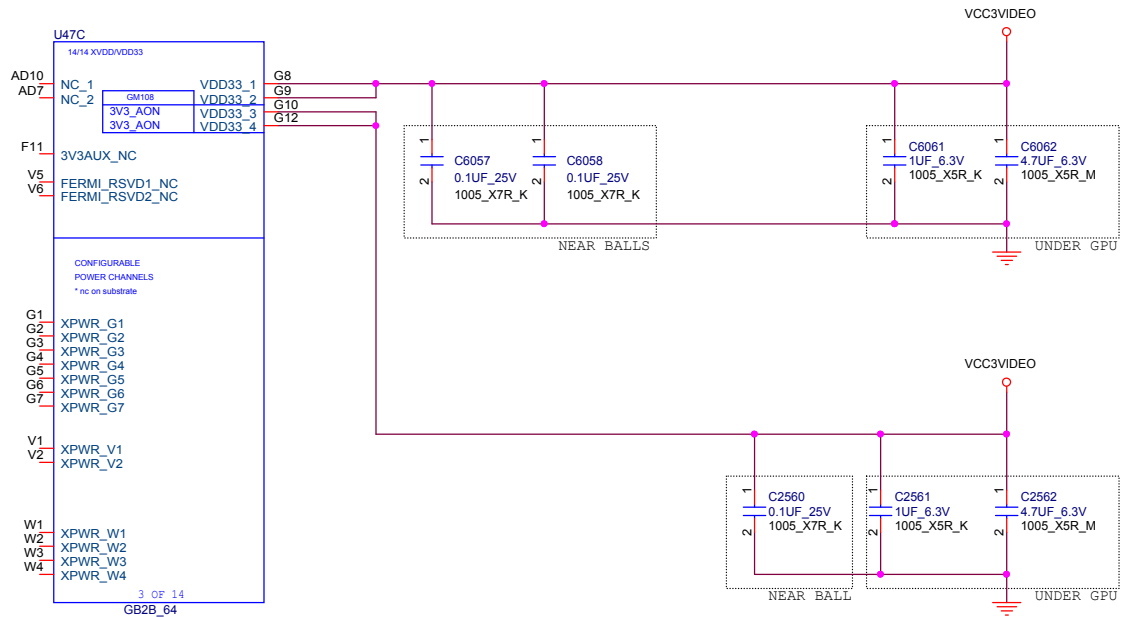
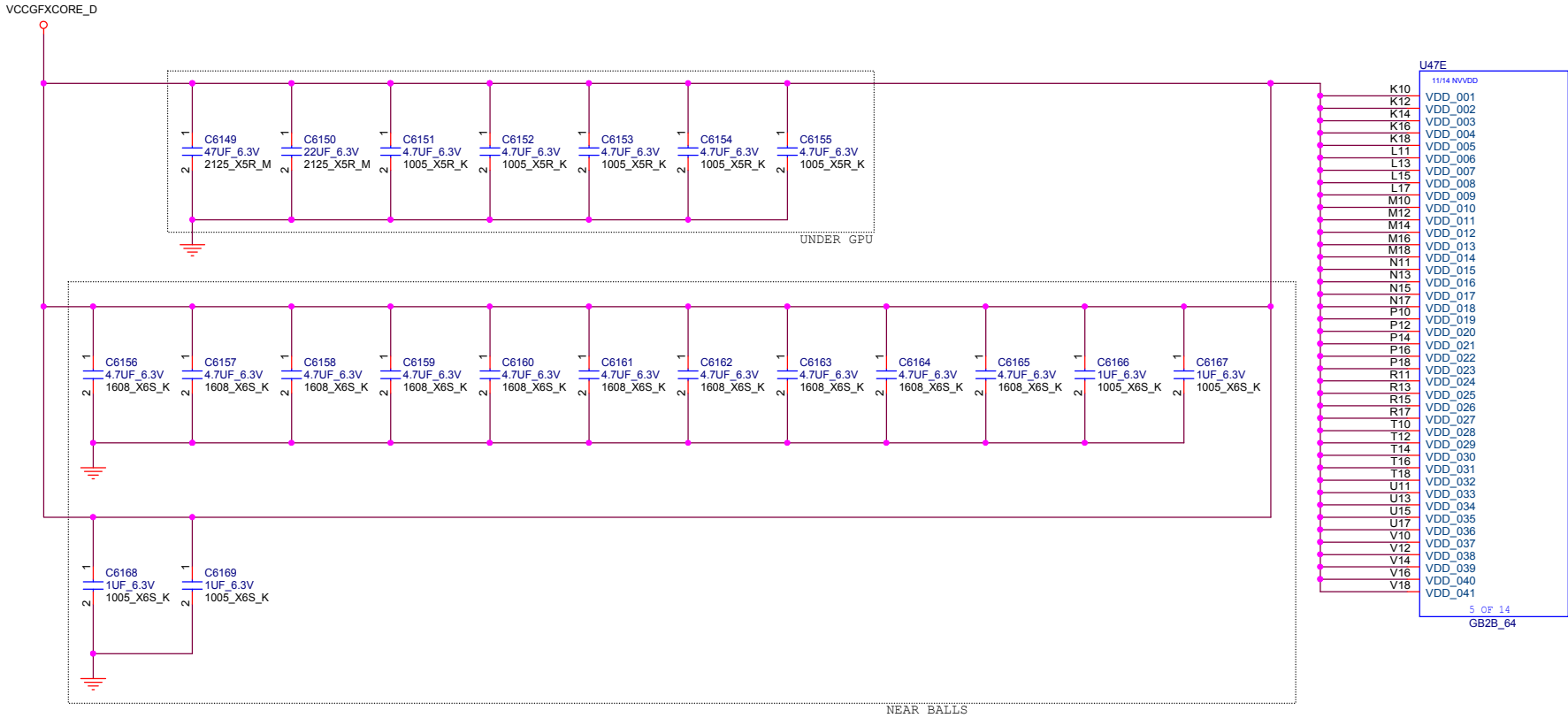


TABLE VIDEO MEMORY

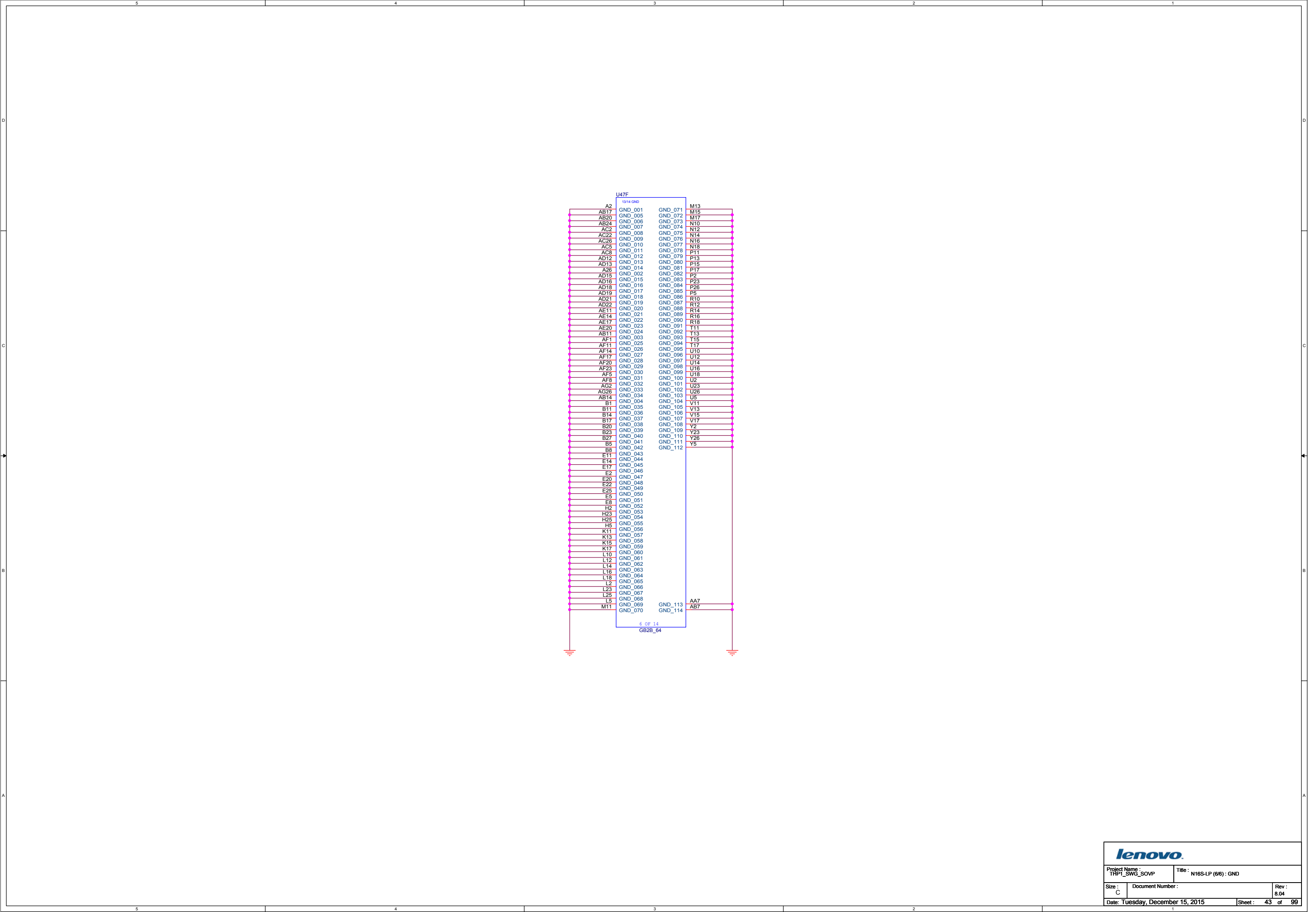
ROM_SIPD	SAMSUNG 256Mx16 Rev.E 0001	HYNIX 256Mx16 Rev.C 0010
R8594	NO_ASM	NO_ASM
R8597	10Kohm	15Kohm

LOGIC



lenovo

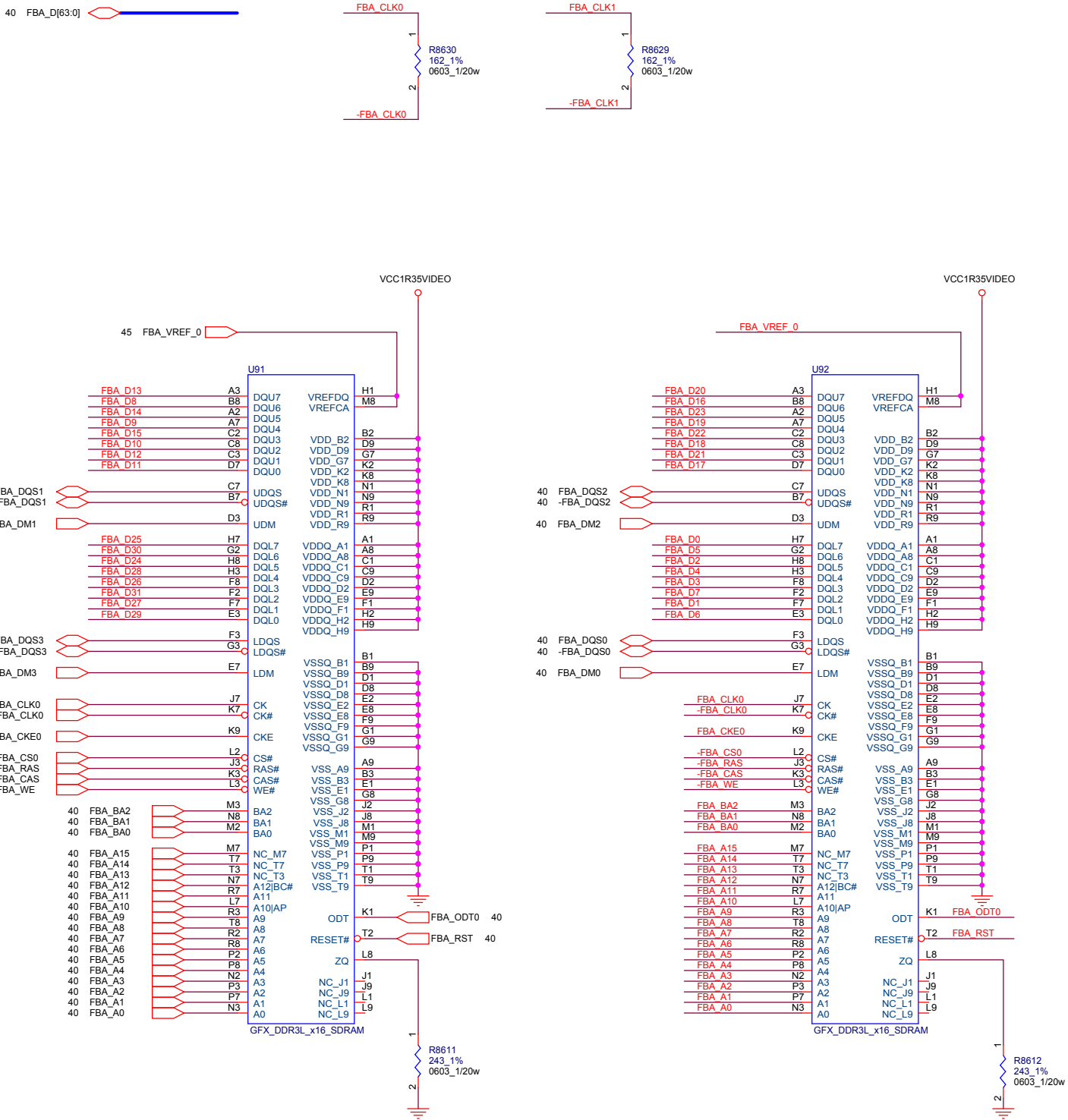
Project Name : THP1_SWG_SOVP
Title : N16S-LP (5/6) : POWER
Size : C
Document Number :
Rev : 8.04
Date: Tuesday, December 15, 2015
Sheet : 42 of 99



Project Name : THP1_SWG_SOVP Title : N16S-LP (6/6) : GND

Size : C Document Number : Rev : 8.04

Date: Tuesday, December 15, 2015 Sheet : 43 of 99



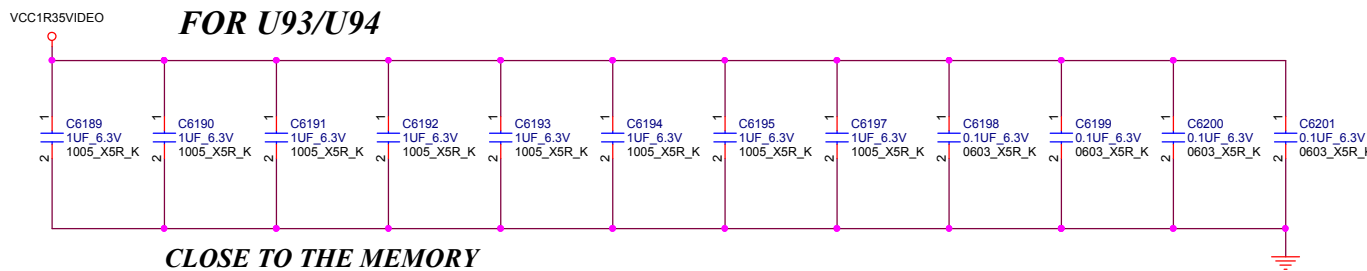
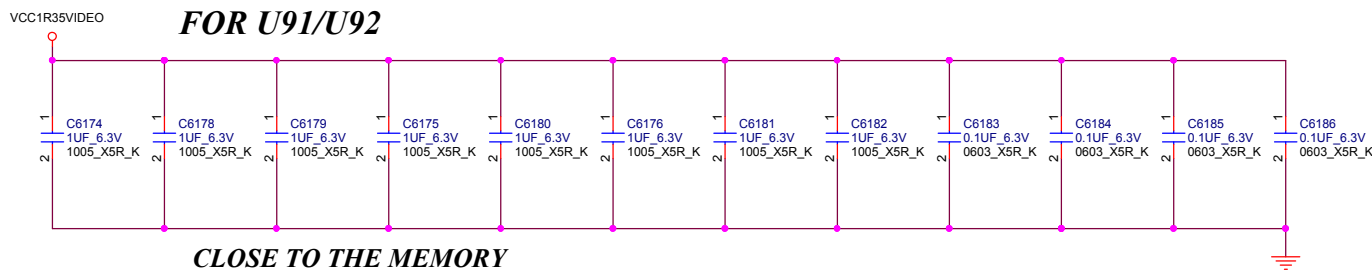
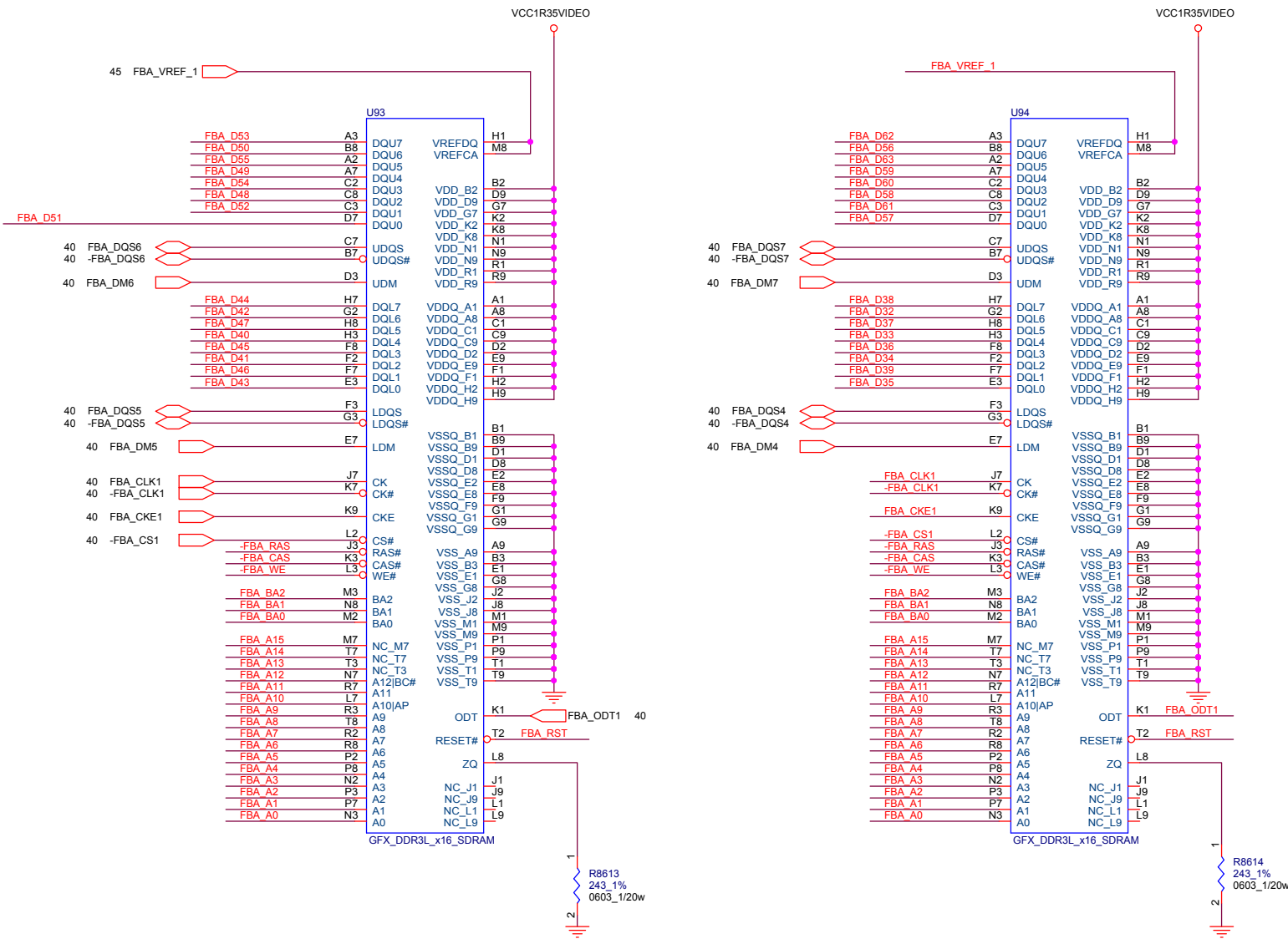
TABLE

DDR3 VIDEO MEMORY

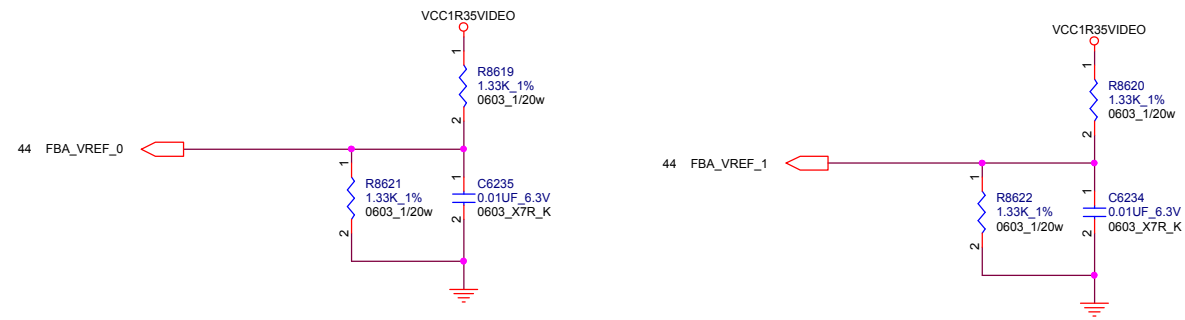
	SAMSUNG 4GBITS (256Mx16)	HYNIX 4GBITS (256Mx16)
U91 U92 U93 U94	K4W4G1646E-BC1A	H5TC4G63CFR-N0C

↑

LOGIC



lenovo



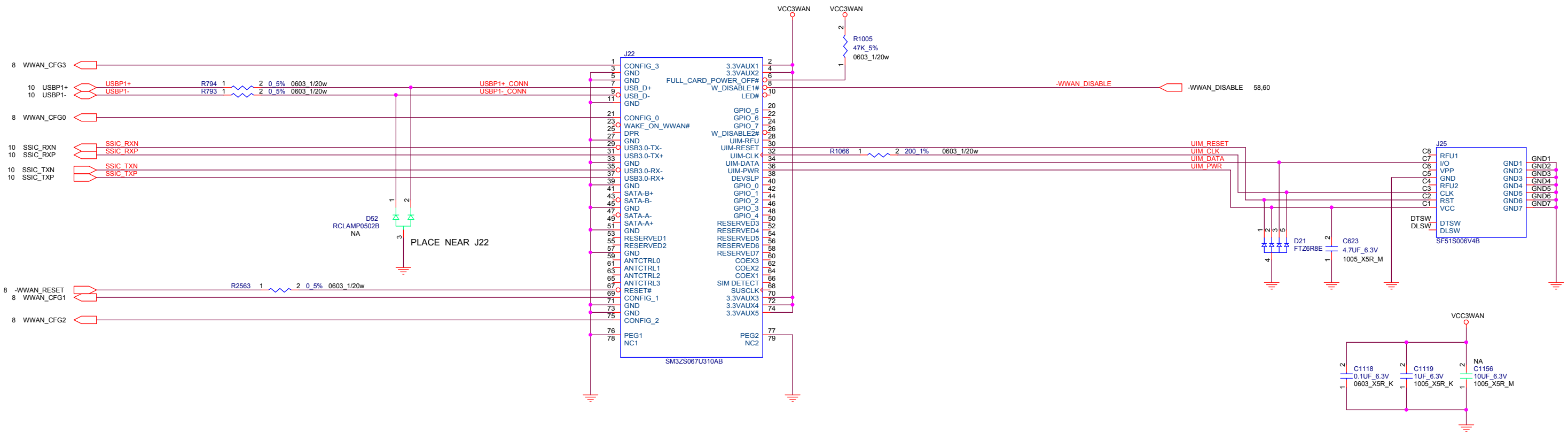
Project Name : THP1_SWG_SOVP Title : MEMORY TERMINATION

Size : C Document Number : Rev : 8.04

Date: Tuesday, December 15, 2015 Sheet : 45 of 99

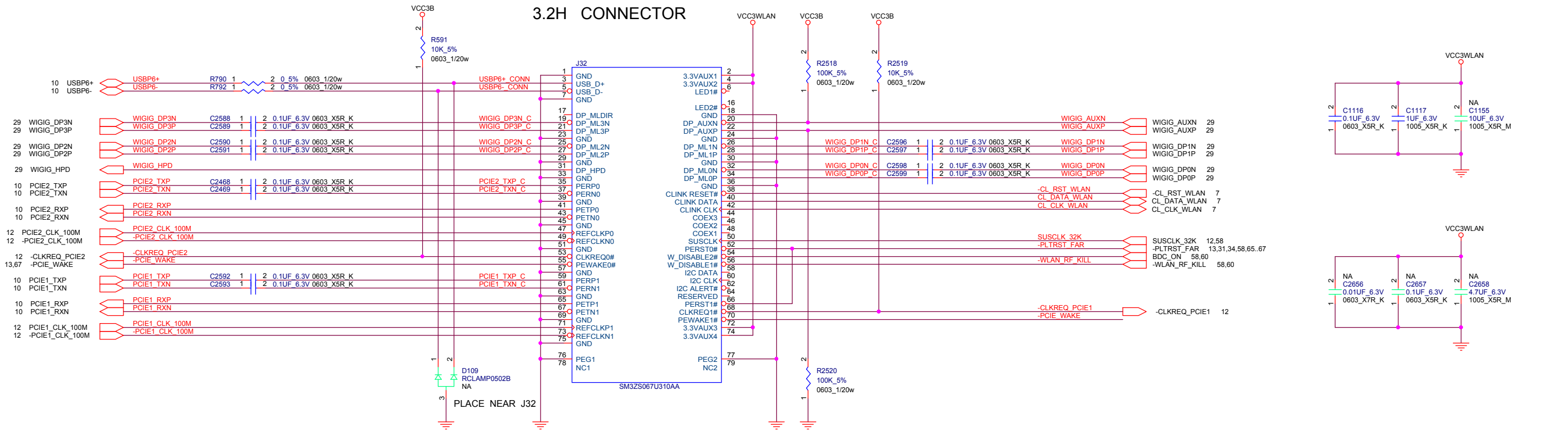
TYPE-B NGFF CARD FOR WWAN

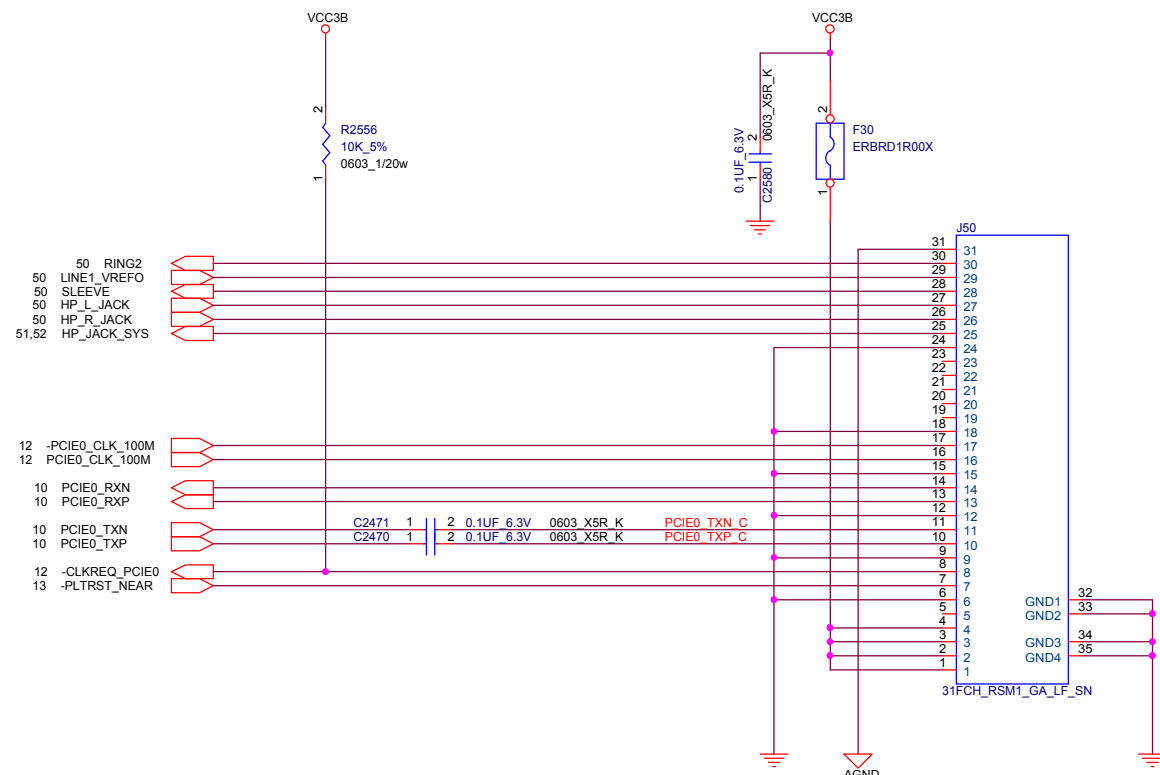
3.2H CONNECTOR



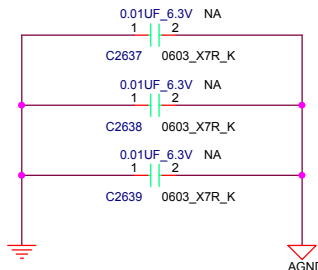
TYPE-A NGFF CARD FOR WLAN

3.2H CONNECTOR





Reserved for EMC/RF solution



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Project Name : THP1_SWG_SOVP		Title : BLANK	
Size : C	Document Number :		Rev : 8.04
Date: Tuesday, December 15, 2015		Sheet :	48 of 99

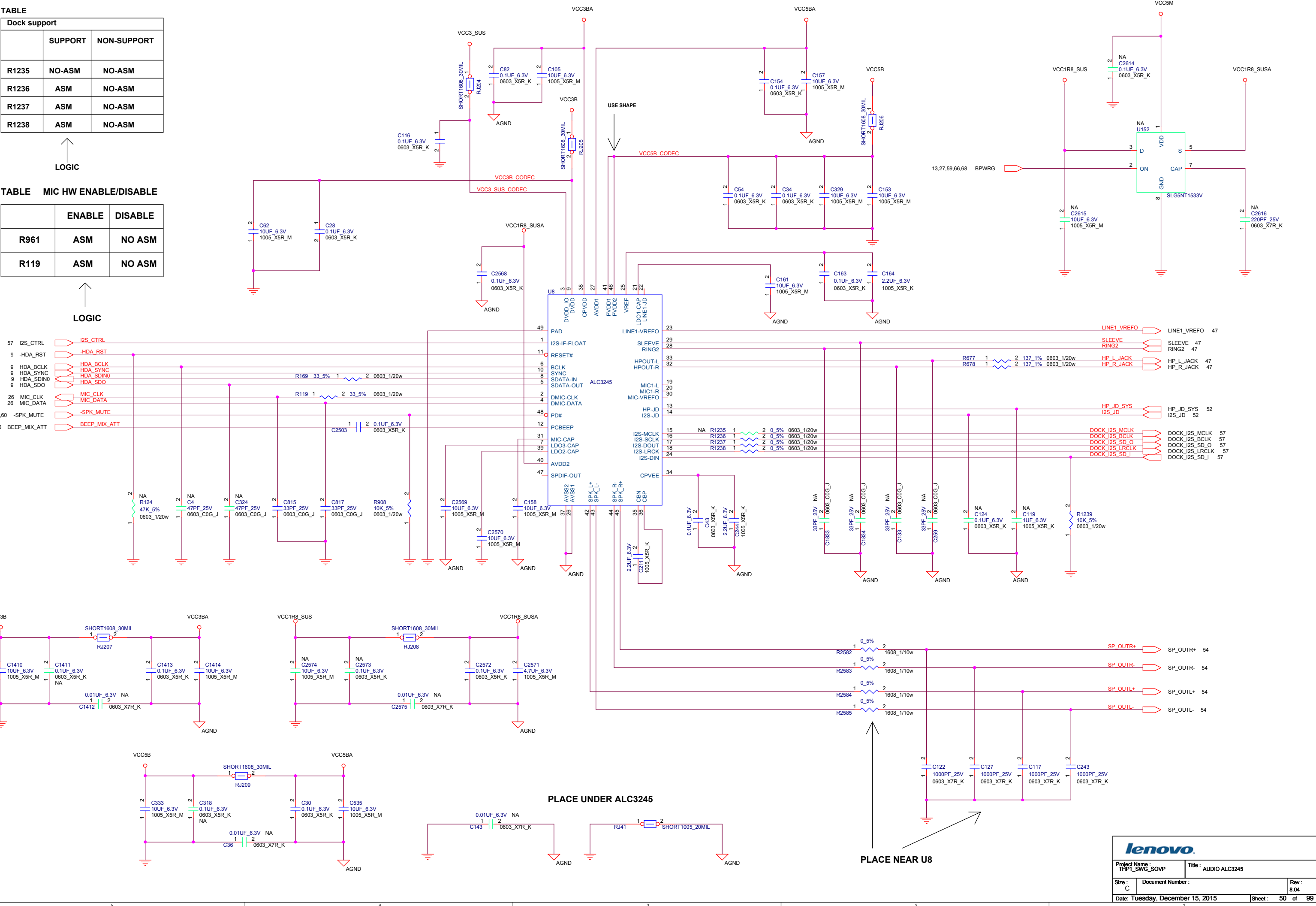
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TABLE

Dock support		
	SUPPORT	NON-SUPPORT
R1235	NO-ASM	NO-ASM
R1236	ASM	NO-ASM
R1237	ASM	NO-ASM
R1238	ASM	NO-ASM

TABLE MIC HW ENABLE/DISABLE

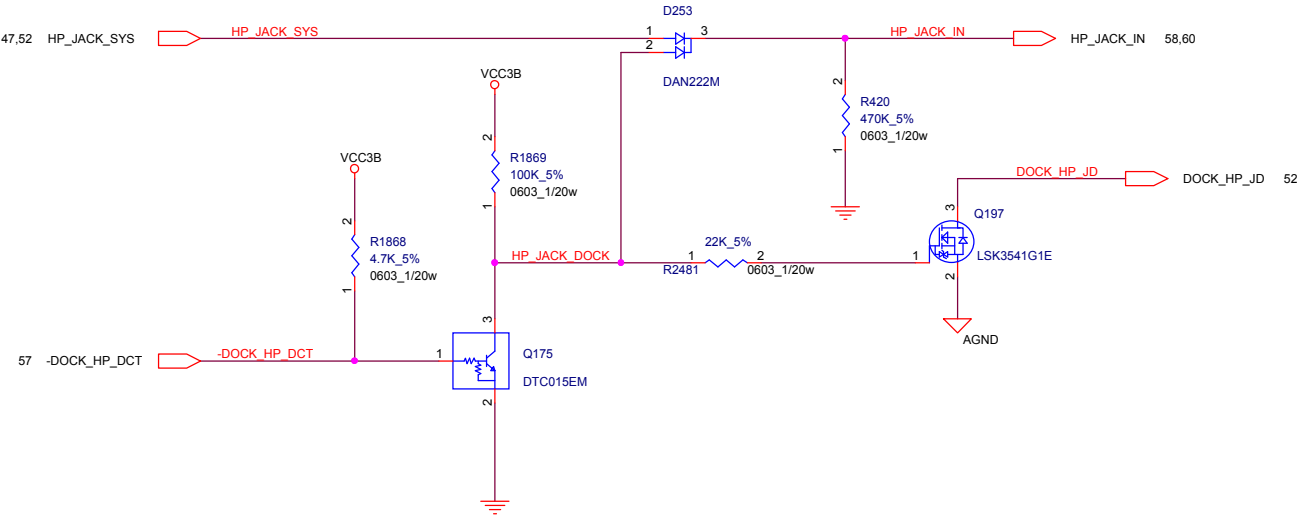
	ENABLE	DISABLE
R961	ASM	NO ASM
R119	ASM	NO ASM

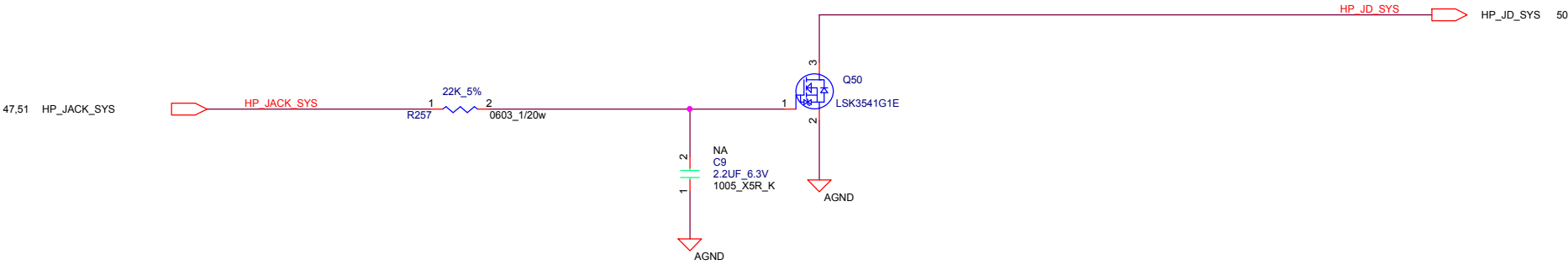
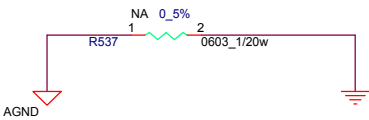


TABLE

DOCKING	SUPPORT	NON-SUPPORT
R1869	ASM	NO_ASM
Q175	ASM	NO_ASM
R2481	ASM	NO_ASM
Q197	ASM	NO_ASM

↑
LOGIC

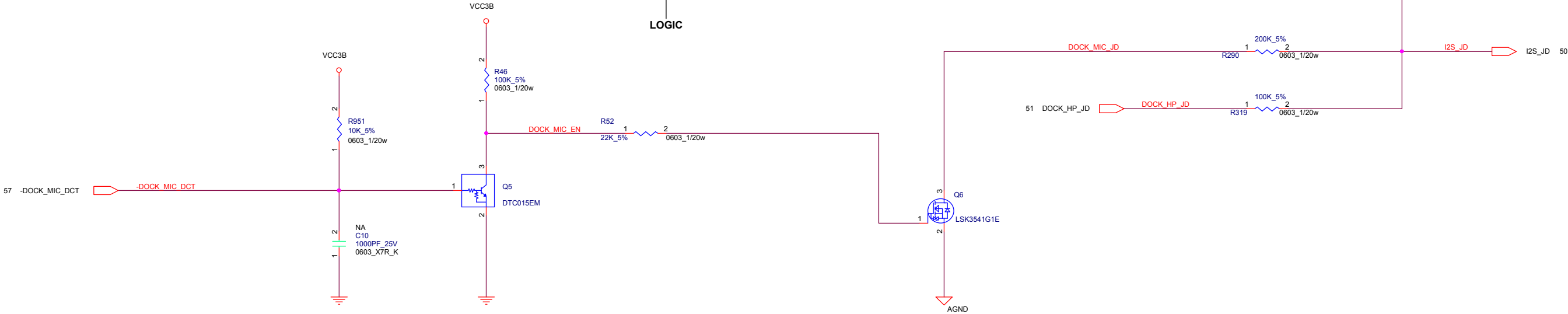




TABLE

DOCKING	SUPPORT		NON-SUPPORT
	ENABLE	DISABLE	
MIC HW			
R951	ASM	NO_ASM	NO_ASM
R290	ASM	NO_ASM	NO_ASM
R46	ASM	NO_ASM	NO_ASM
Q5	ASM	NO_ASM	NO_ASM
R52	ASM	NO_ASM	NO_ASM
Q6	ASM	NO_ASM	NO_ASM
R319	ASM	ASM	NO_ASM
R2572	ASM	ASM	ASM

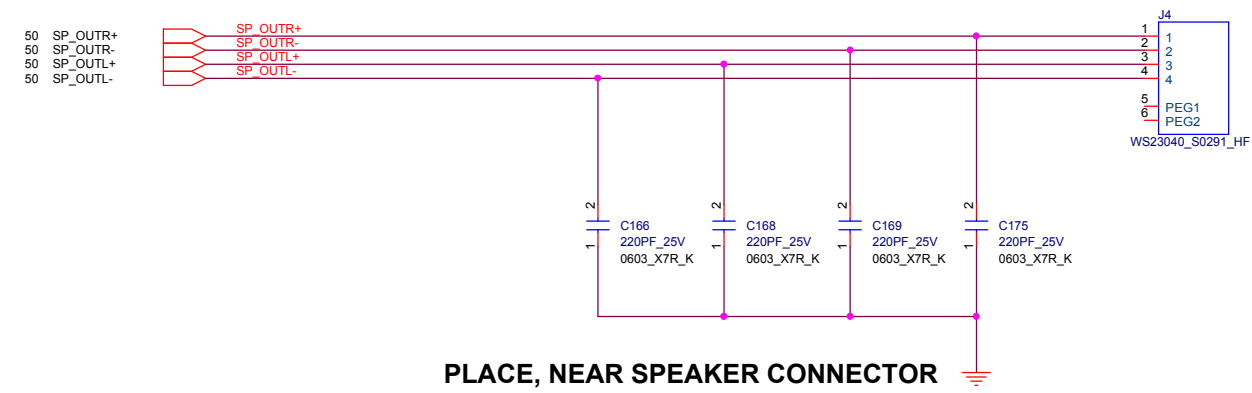
LOGIC

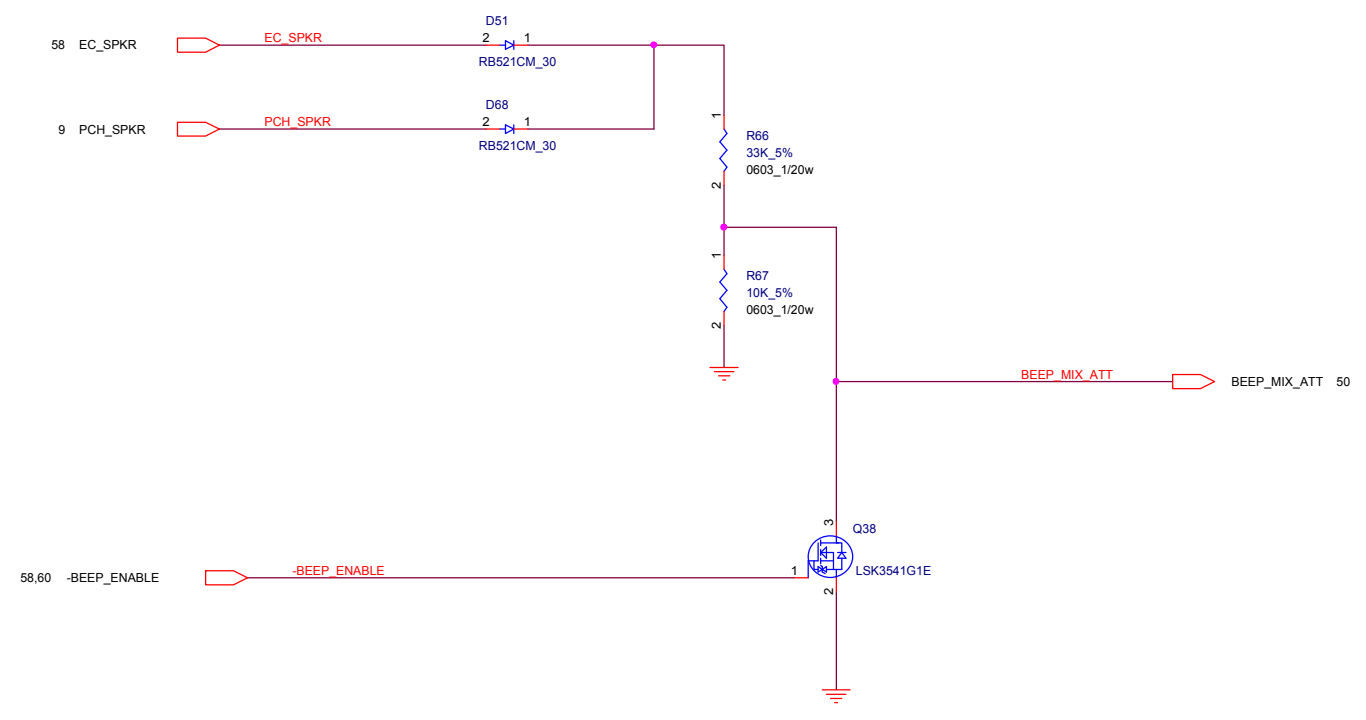


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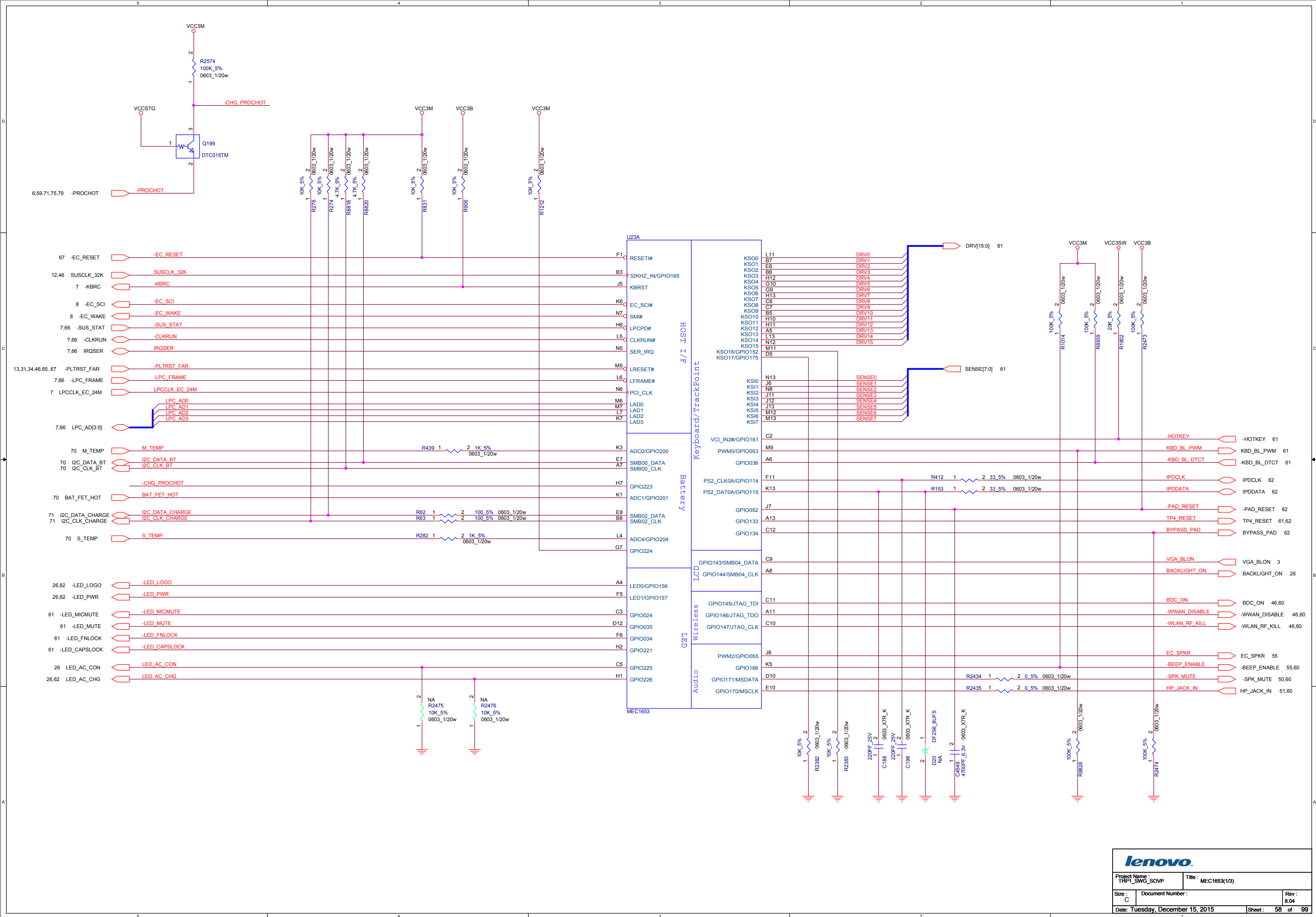


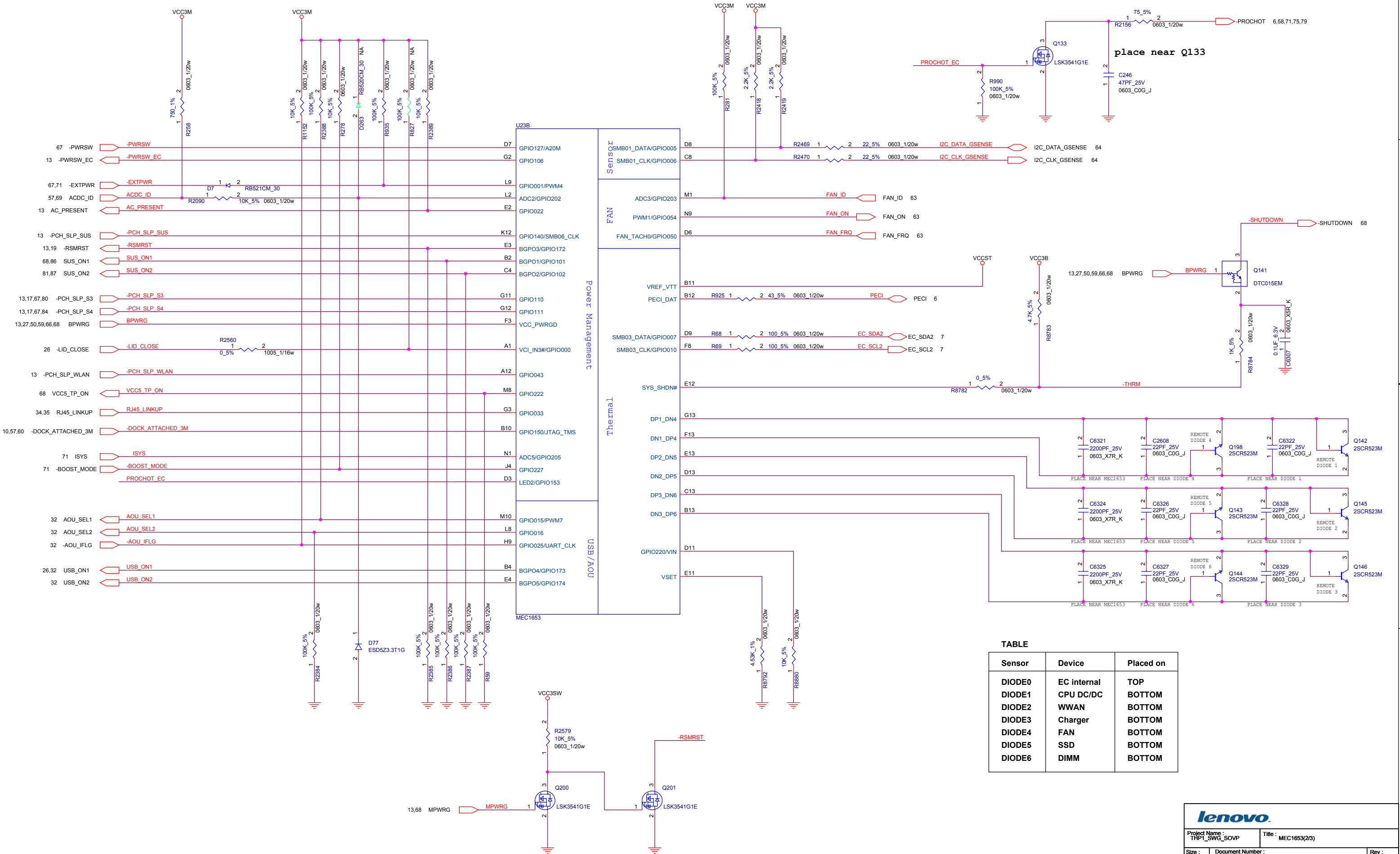
Project Name : THP1_SWG_SOVP		Title : BLANK	
Size : C	Document Number :		Rev : 8.04
Date: Tuesday, December 15, 2015		Sheet :	53 of 99





BLANK





Sensor	Device	Placed on
DIODE0	EC internal	TOP
DIODE1	CPU DC/DC	BOTTOM
DIODE2	WWAN	BOTTOM
DIODE3	Charger	BOTTOM
DIODE4	FAN	BOTTOM
DIODE5	SSD	BOTTOM
DIODE6	DIMM	BOTTOM

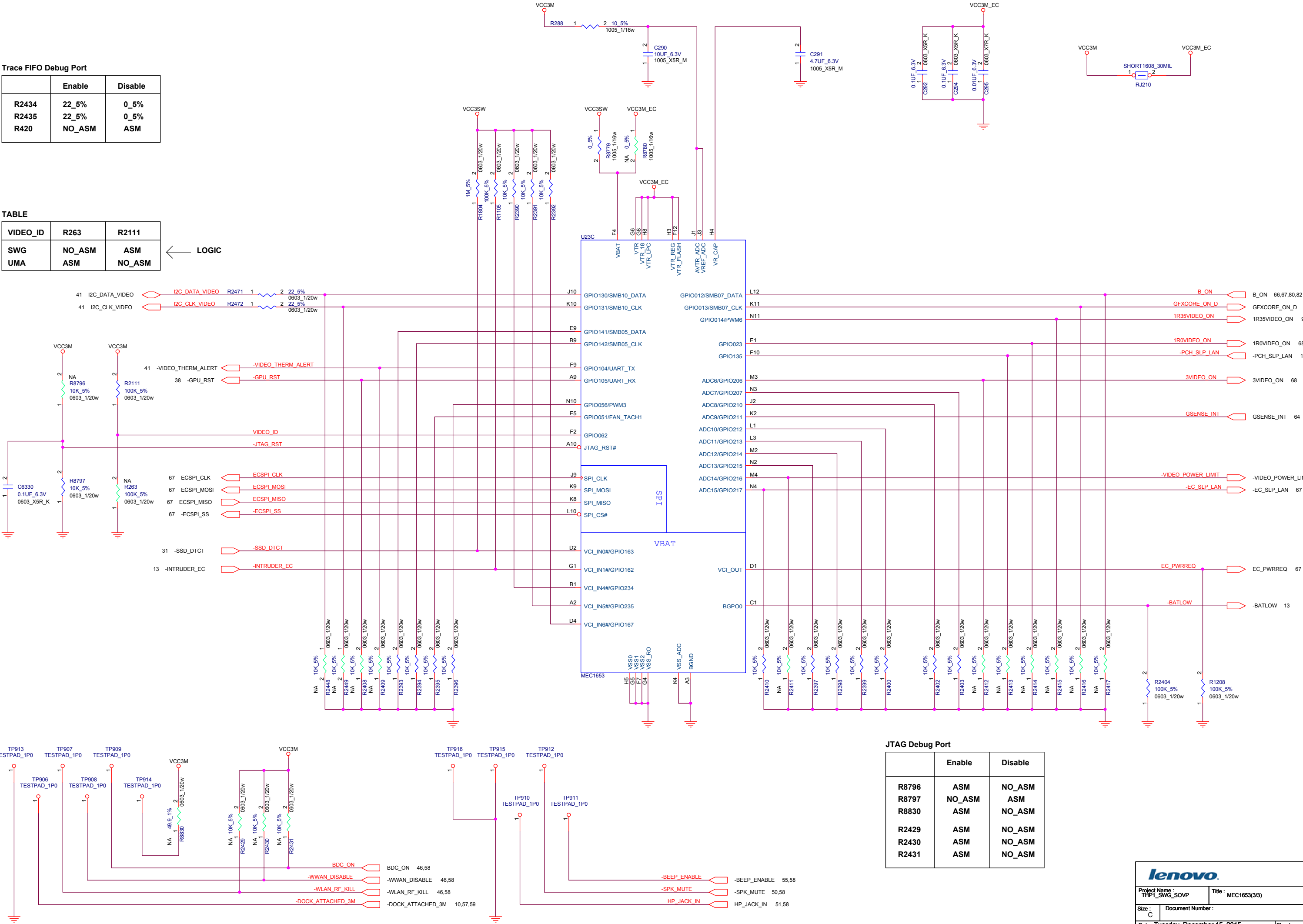
Trace FIFO Debug Port

	Enable	Disable
R2434	22_5%	0_5%
R2435	22_5%	0_5%
R420	NO_ASM	ASM

TABLE

VIDEO_ID	R263	R2111
SWG	NO_ASM	ASM
UMA	ASM	NO_ASM

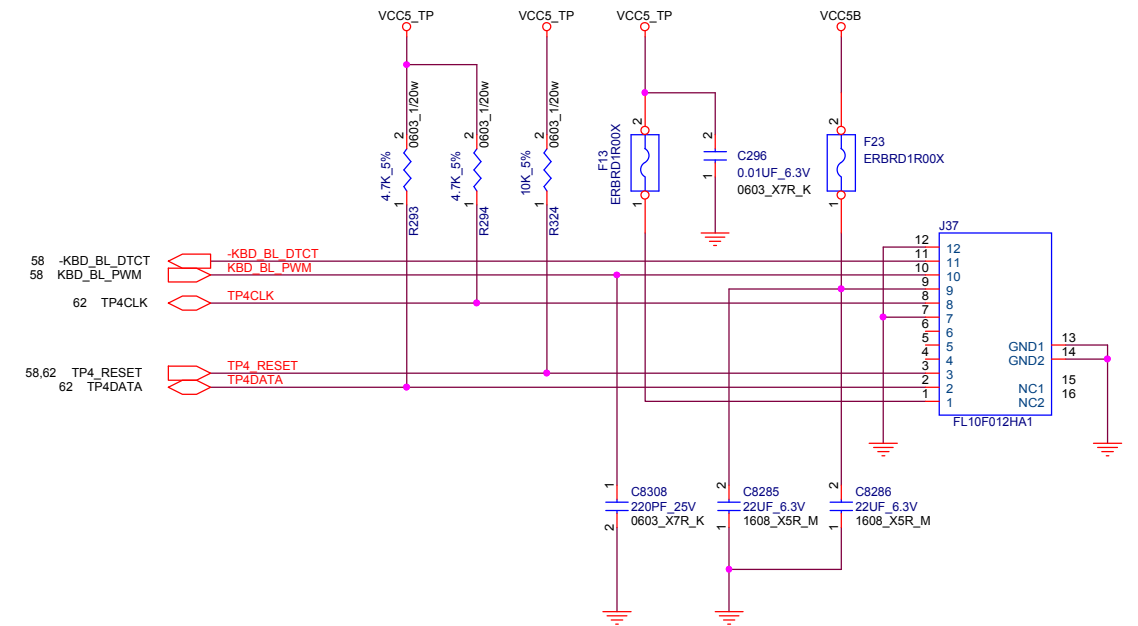
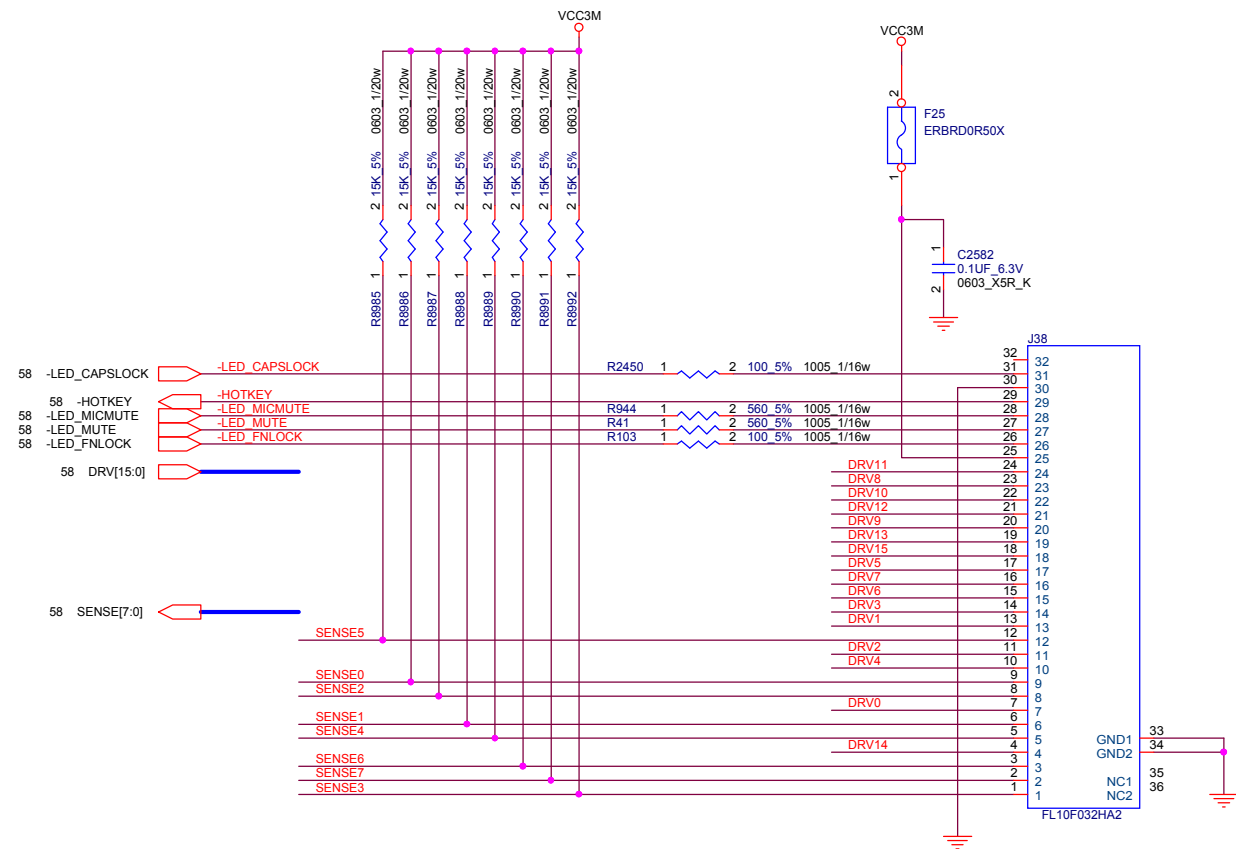
LOGIC

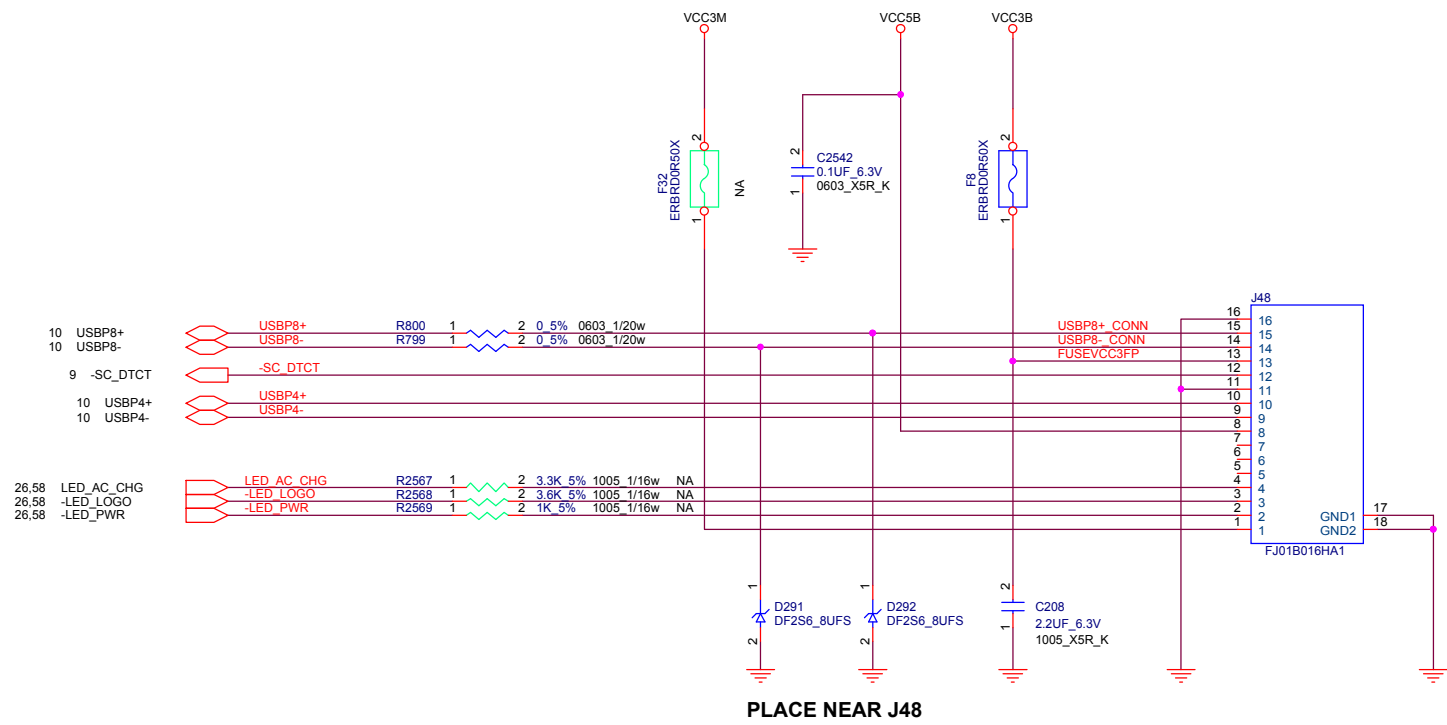
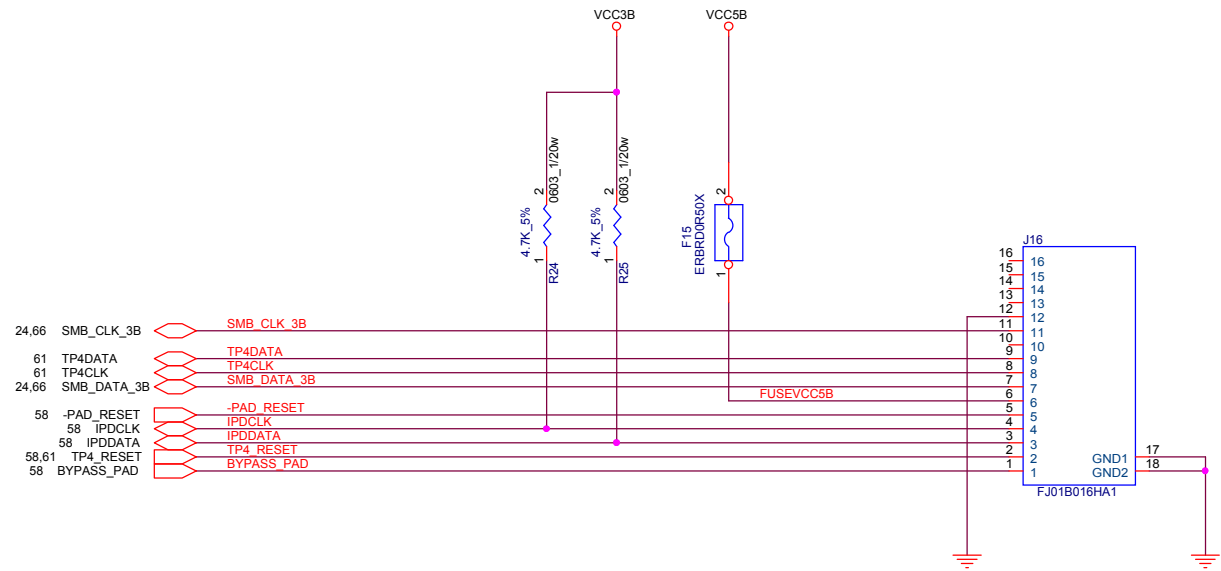


JTAG Debug Port

	Enable	Disable
R8796	ASM	NO_ASM
R8797	NO_ASM	ASM
R8830	ASM	NO_ASM
R2429	ASM	NO_ASM
R2430	ASM	NO_ASM
R2431	ASM	NO_ASM



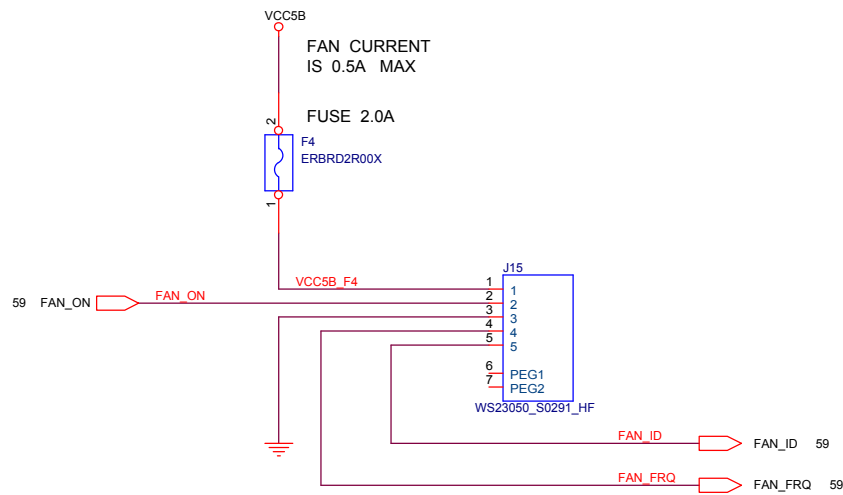




Project Name : THP1_SWG_SOVP Title : TOUCH PAD/FPR/SCR

Size : C Document Number : Rev : 8.04

Date: Tuesday, December 15, 2015 Sheet : 62 of 99

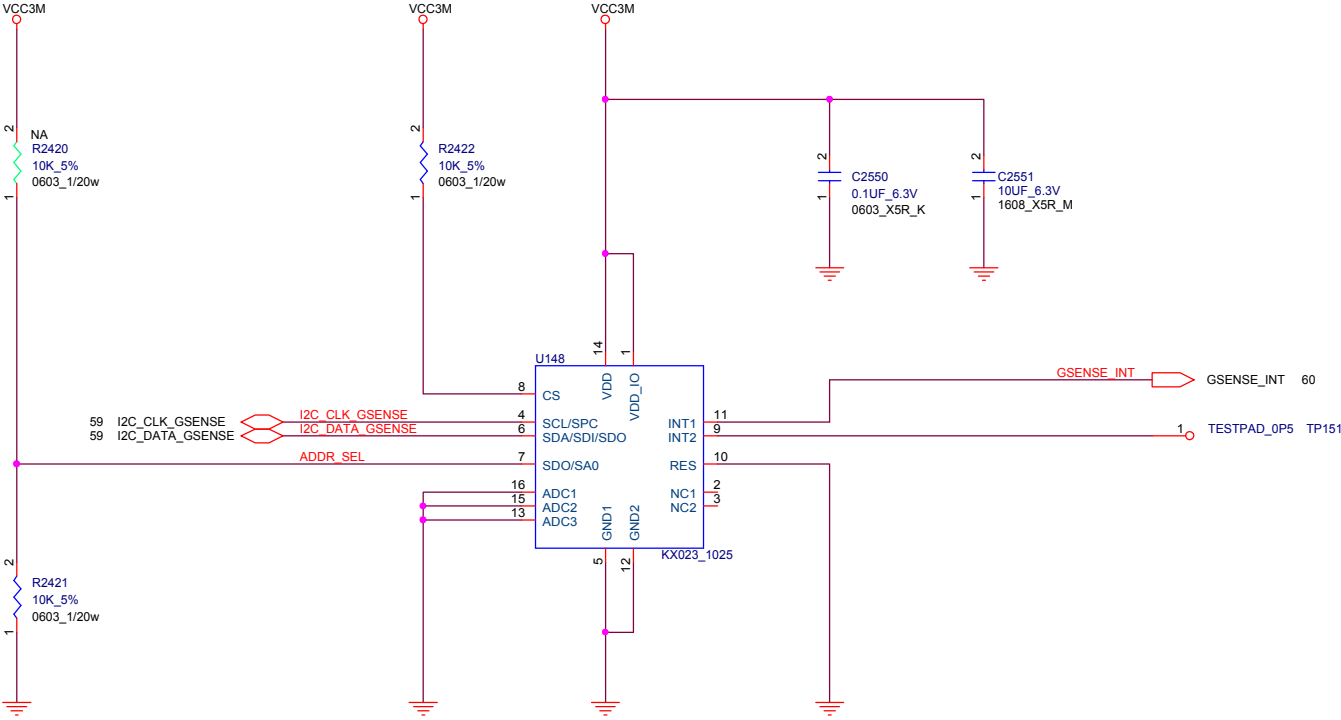


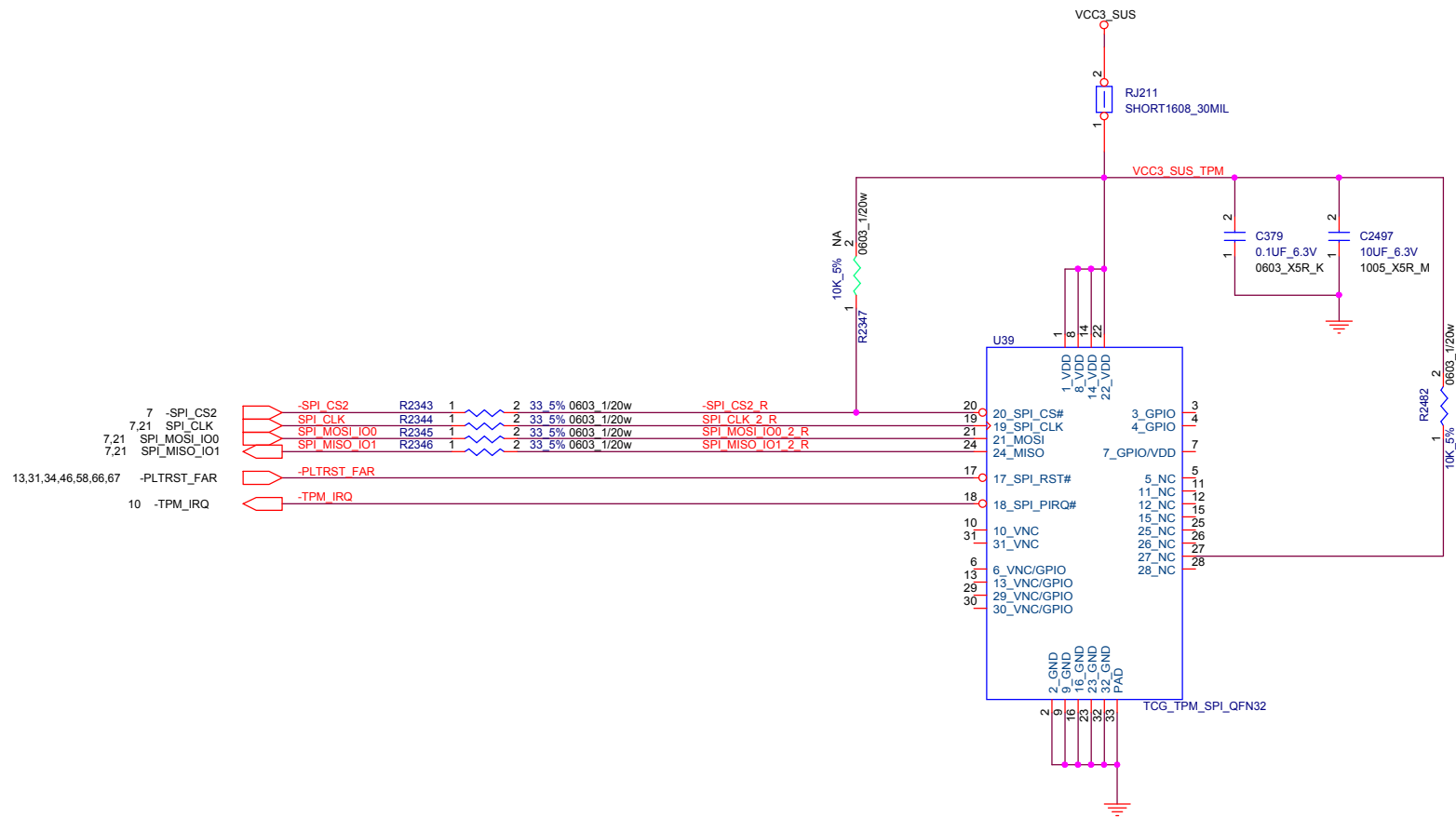
TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode

TABLE

P/N	ADDR_SEL	Address
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)





TABLE

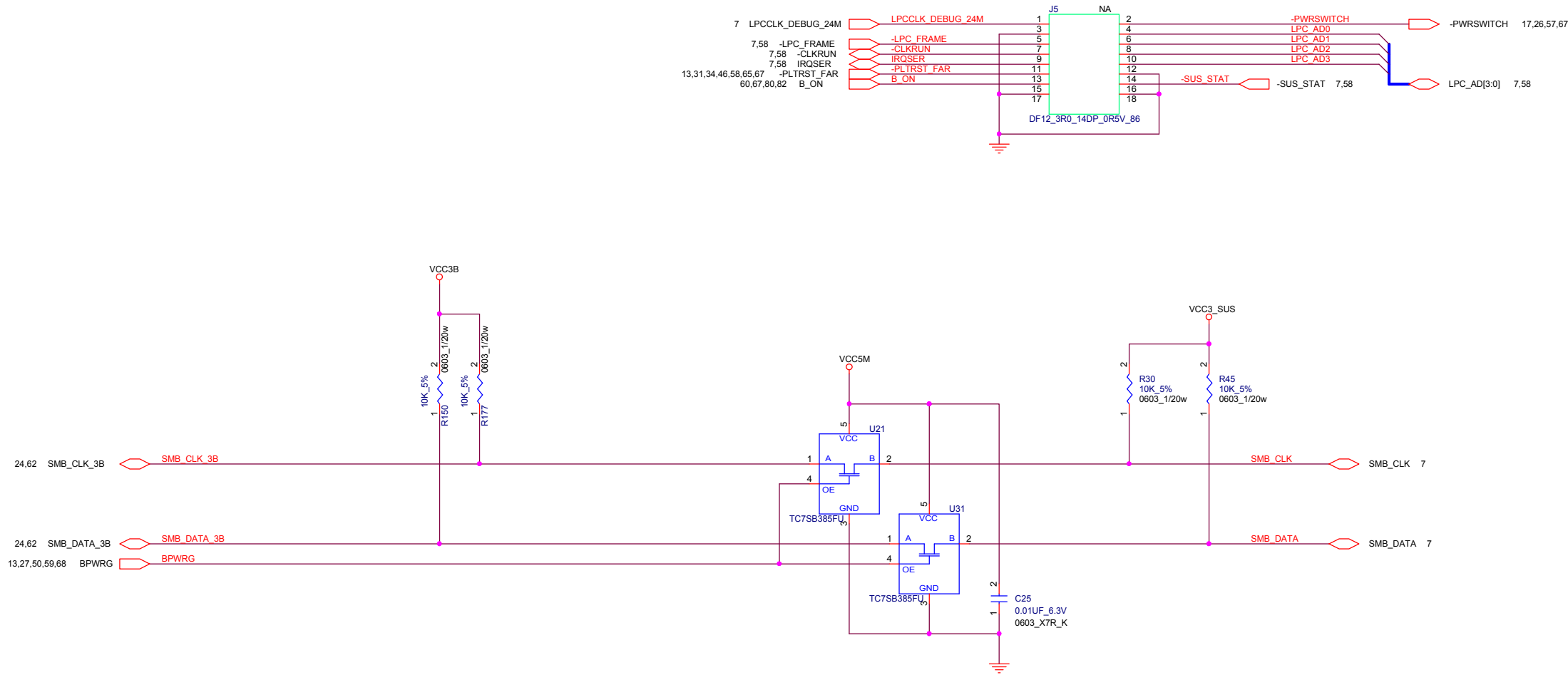
Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.40	ST Micro ST33HTPH2E32AAE5	Nuvoton T.B.D.
1	VDD	VDD	NC	VSB
2	GND	GND	NC	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

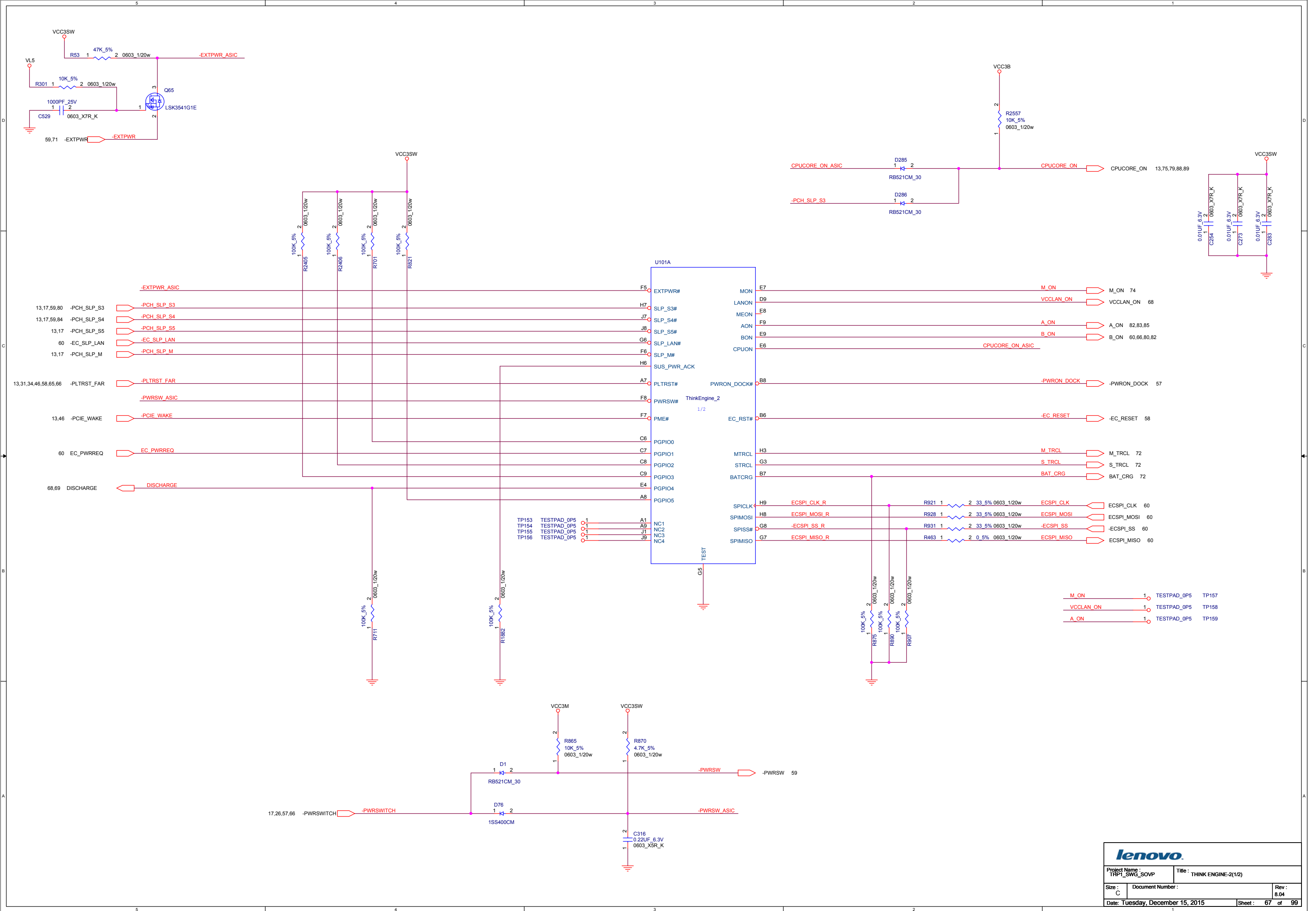


TABLE

REF DES	ENABLE	DISABLE
J5	ASM	NO_ASM
R220	ASM	NO_ASM

LOGIC

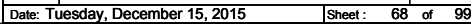




Project Name : THP1_SWG_SOVP Title : THINK ENGINE-2(1/2)

Size : C Document Number : Rev : 8.04

Date : Tuesday, December 15, 2015 Sheet : 67 of 99



DCIN

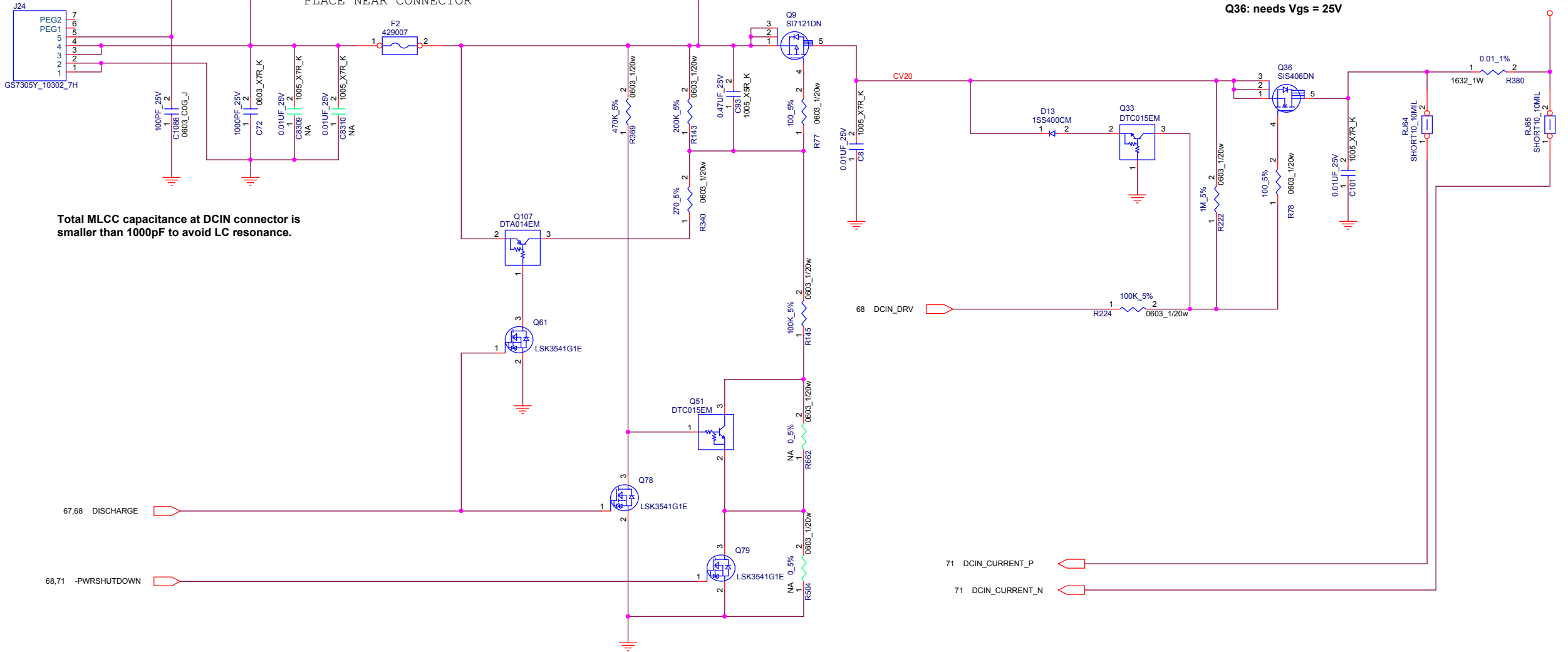
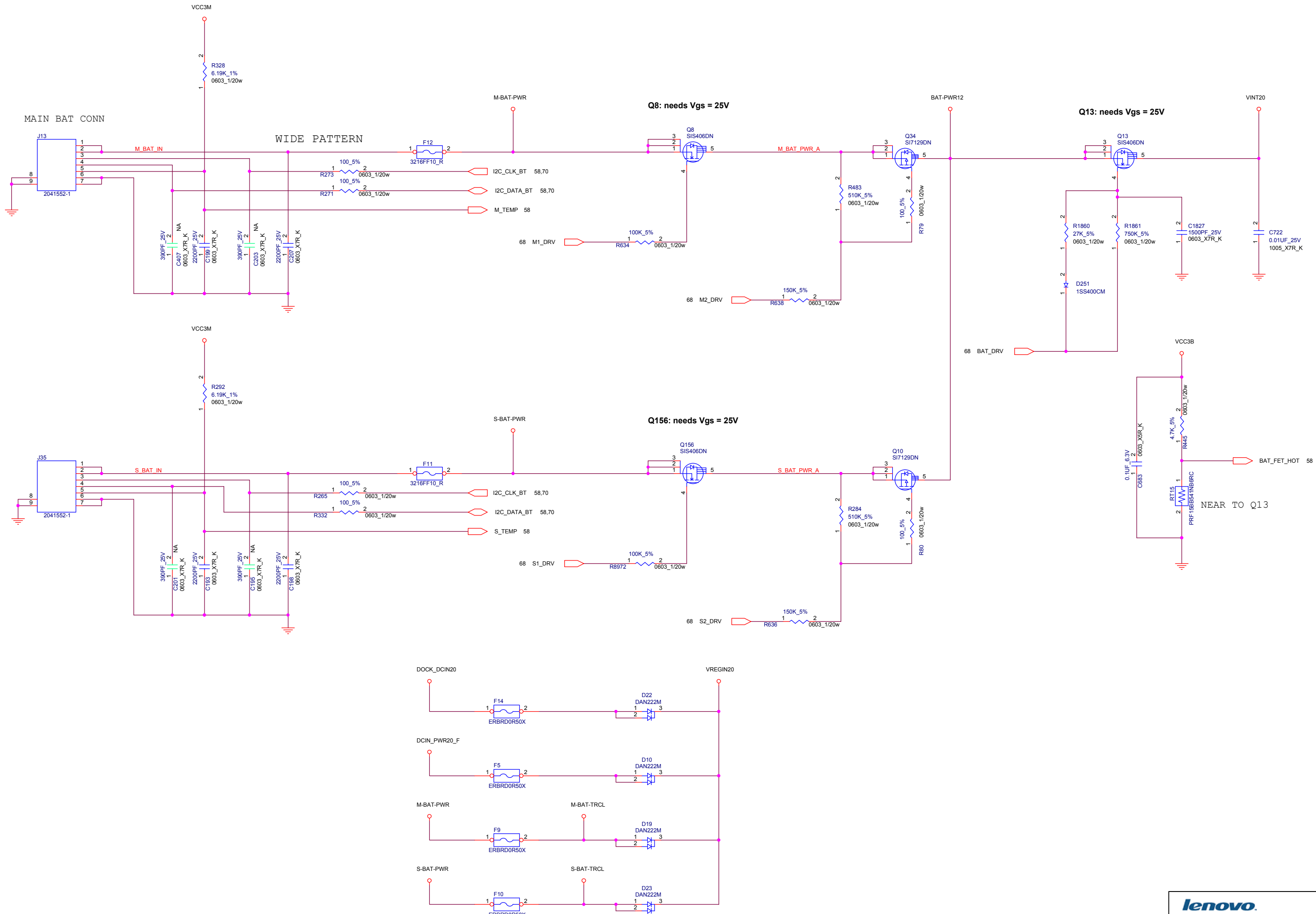
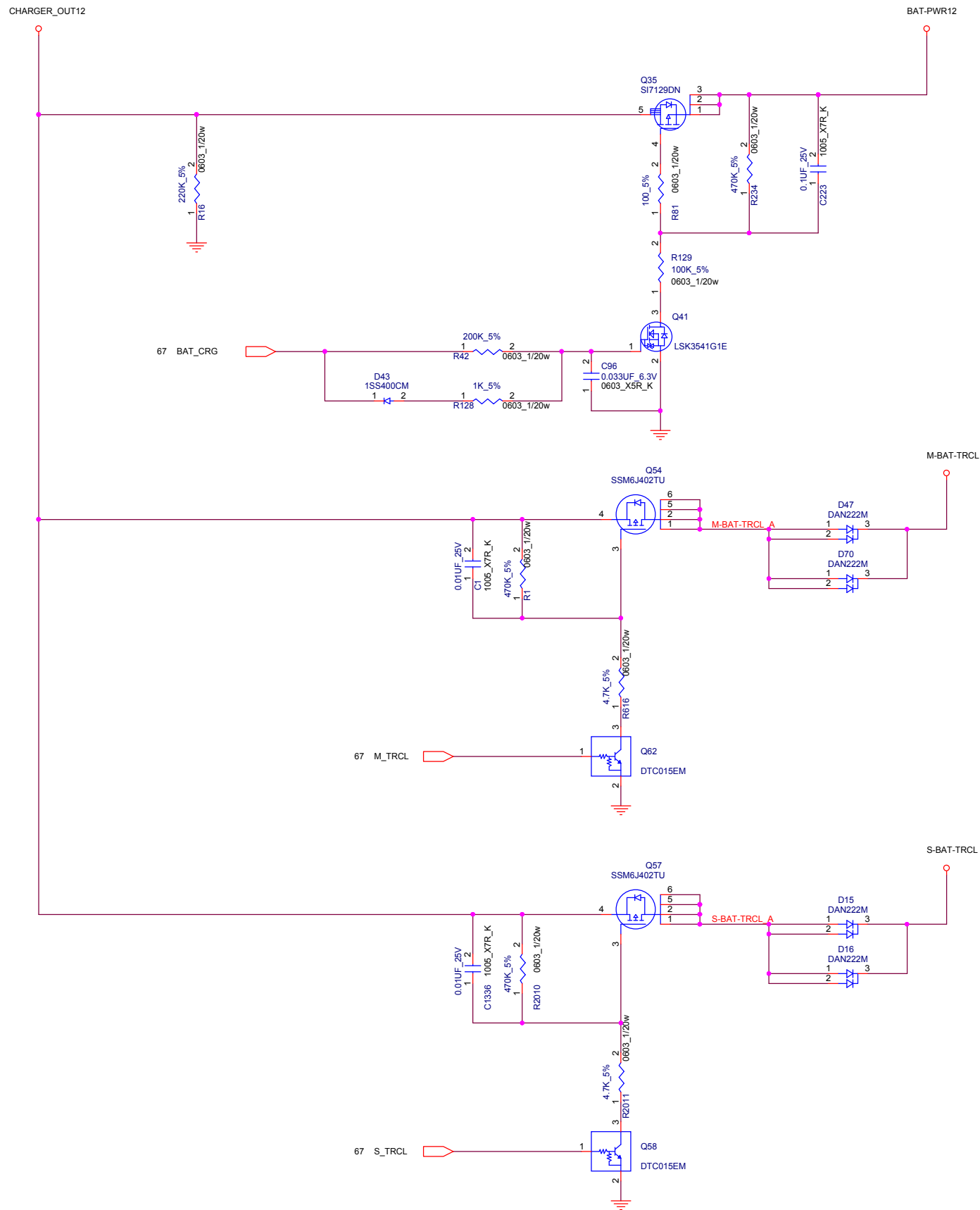


TABLE		
PEAK SHIFT	YES	NO
R662	NO-ASM	ASM
R369	ASM	NO-ASM
Q78	ASM	NO-ASM
Q51	ASM	NO-ASM

↑
LOGIC





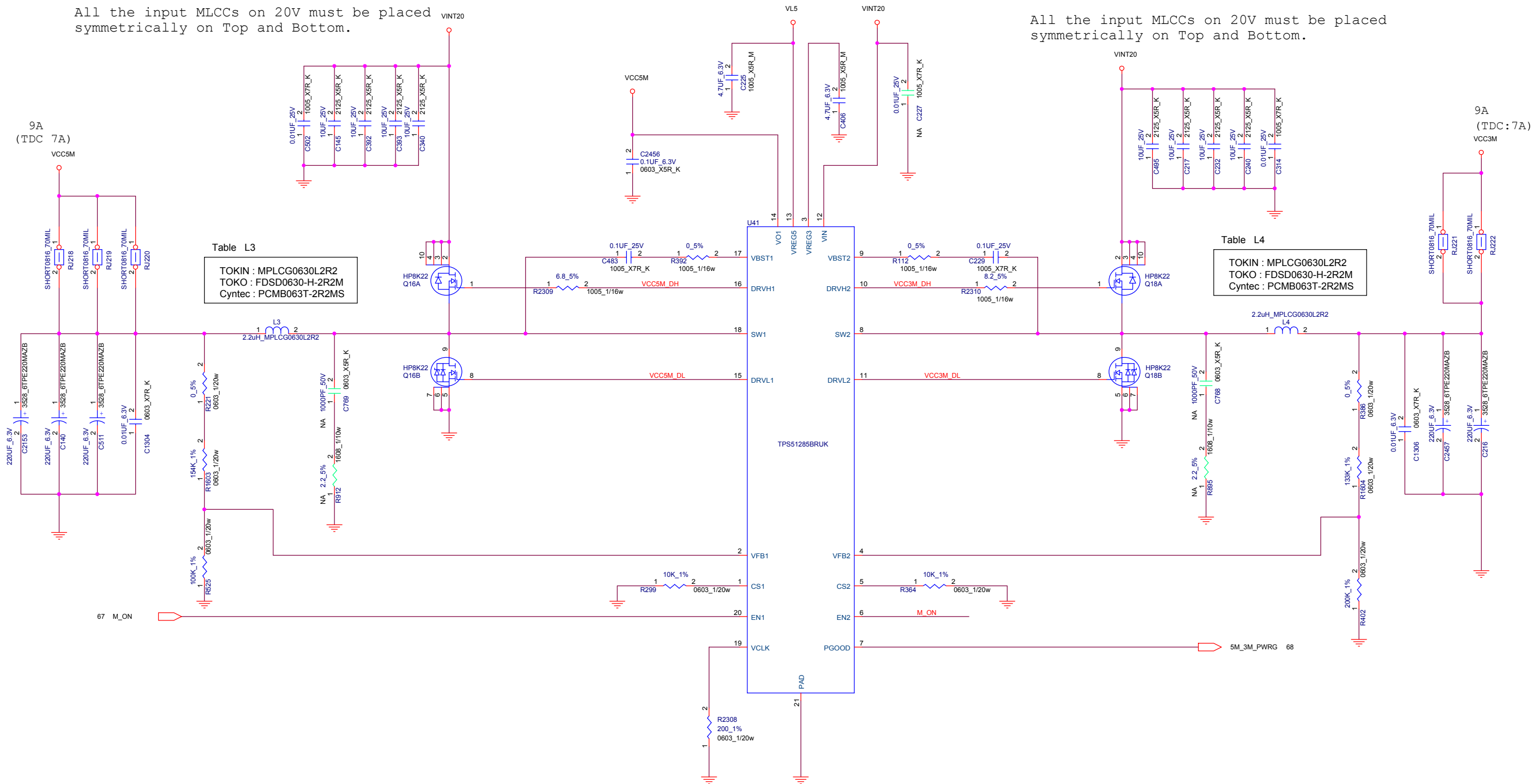
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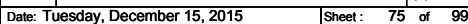


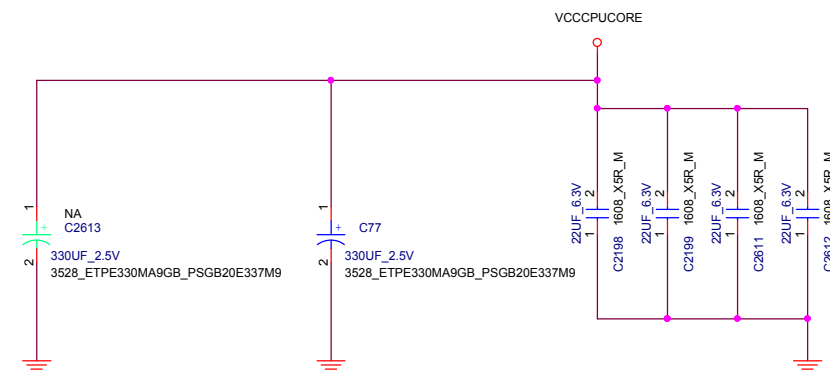
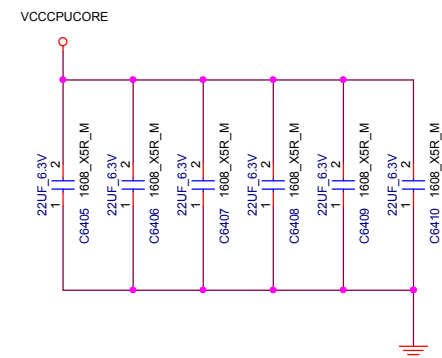
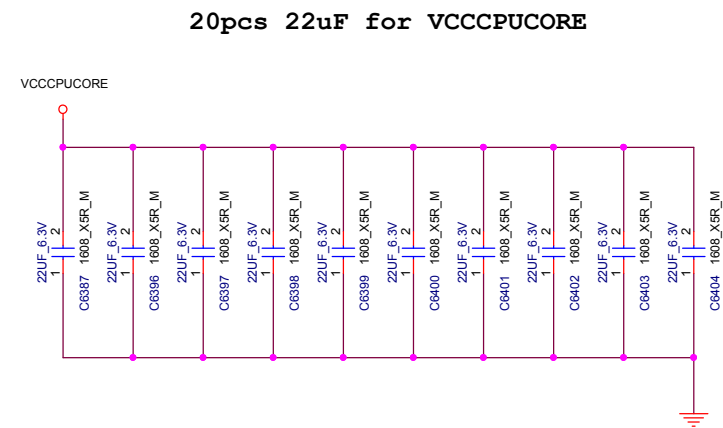
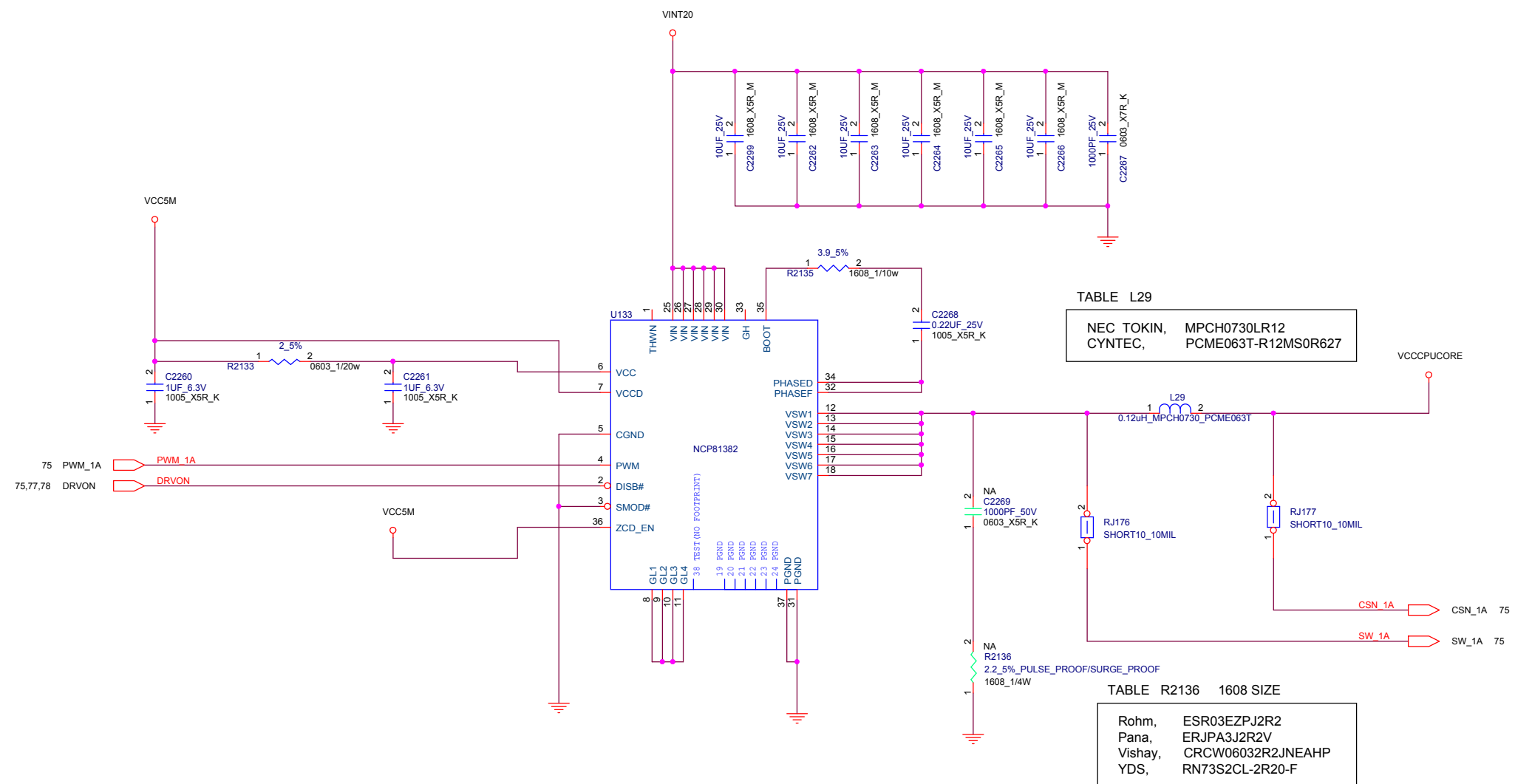
Project Name : THP1_SWG_SOVP		Title : BLANK	
Size : C	Document Number :		Rev : 8.04
Date: Tuesday, December 15, 2015		Sheet : 73 of 99	

All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.







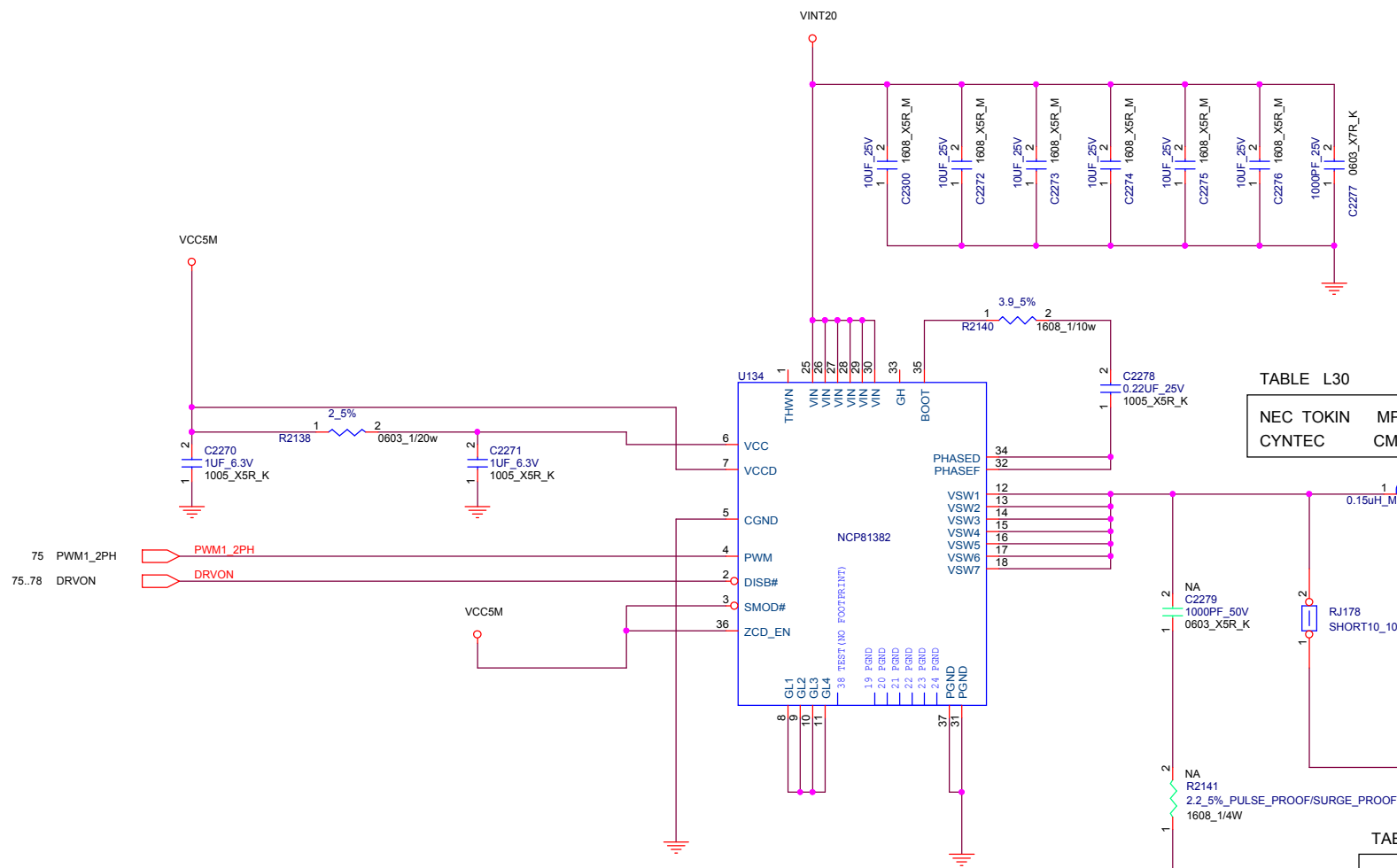


TABLE L30

NEC TOKIN	MPCH0730LR15
CYNTEC	CMLE063T-R15MS0R987-88

TABLE R2141 1608 SIZE

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
Vishay,	CRCW06032R2JNEAHP
YDS,	RN73S2CL-2R20-F

Table for C2508:

Panasonic,	ETPE330MA9GB
NEC TOKIN,	PSGB20E337M9

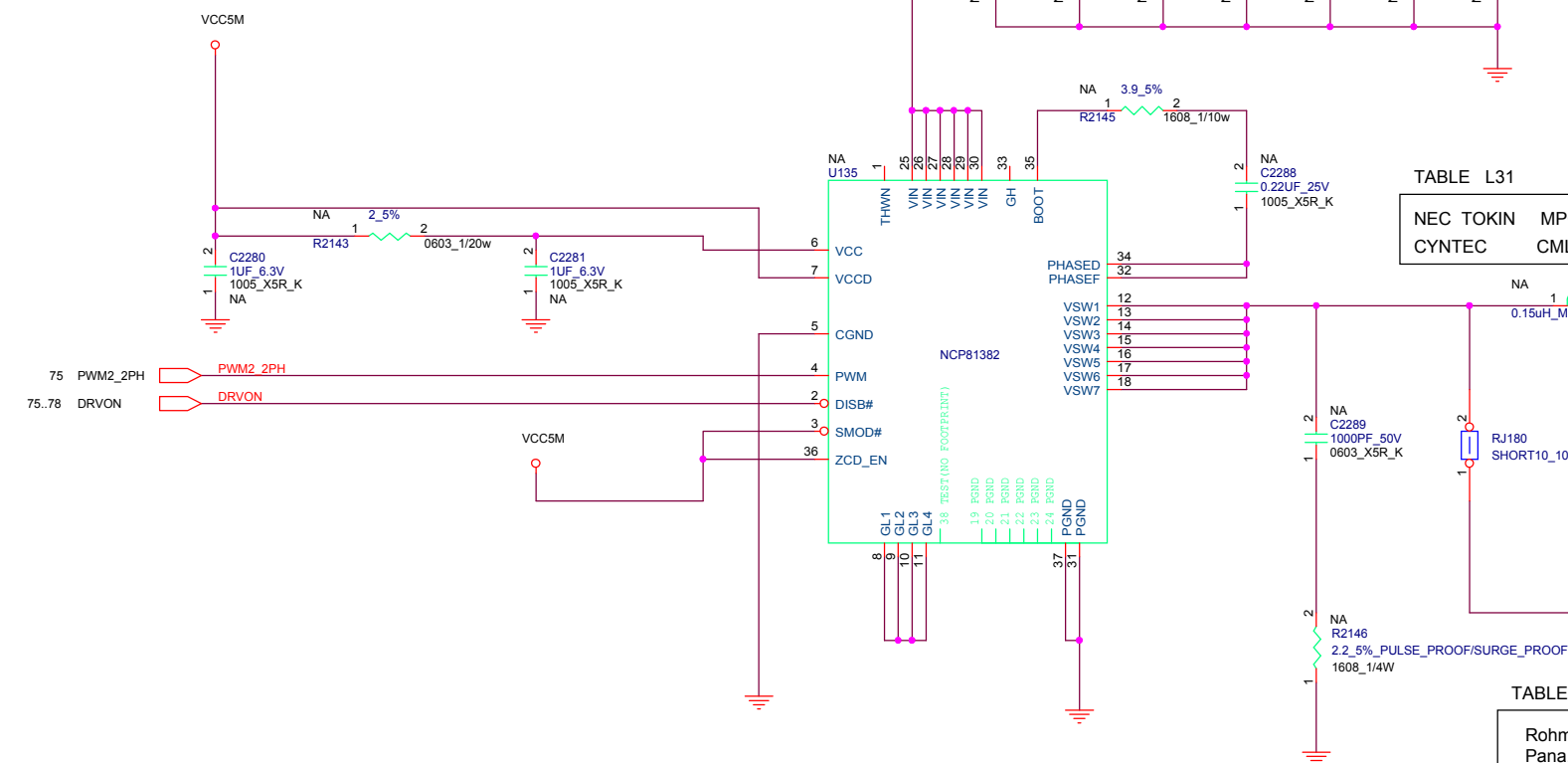
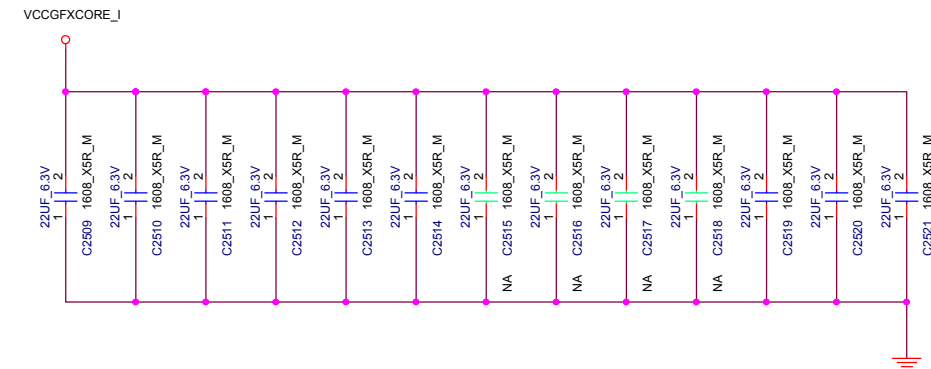


TABLE L31

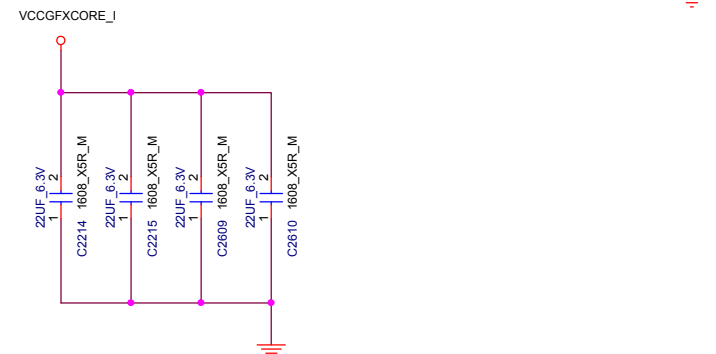
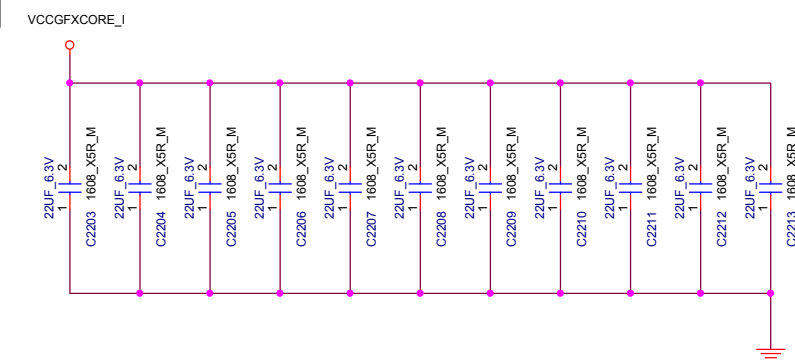
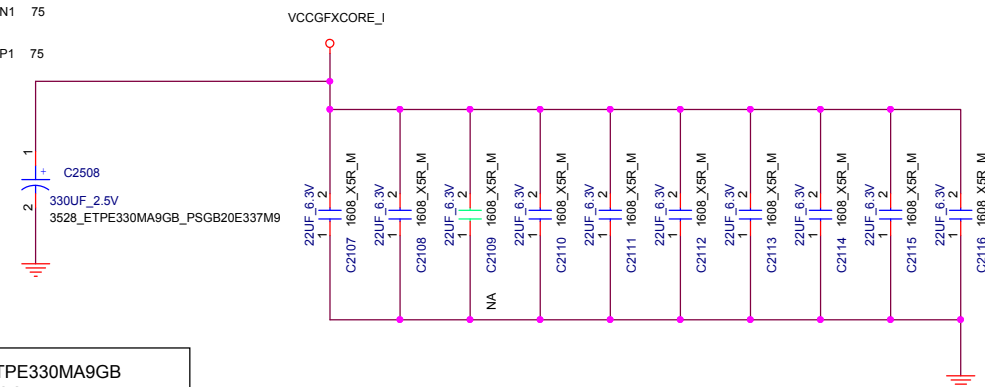
NEC TOKIN	MPCH0730LR15
CYNTEC	CMLE063T-R15MS0R987-88

TABLE R2146 1608 SIZE

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
Vishay,	CRCW06032R2JNEAHP
YDS,	RN73S2CL-2R20-F



33pcs 22uF for VCCGFXCORE_I



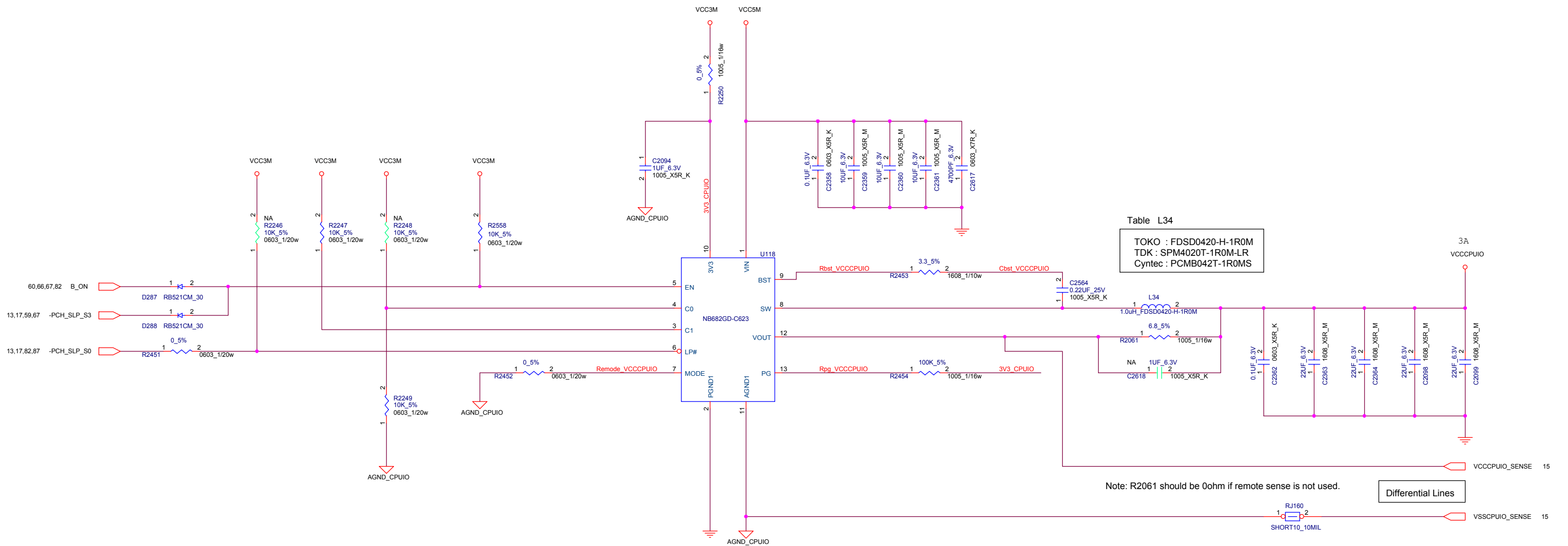


TABLE : NB682 MODE M1 (0 to GND)

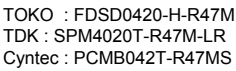
LP#	C1	C0	VOUT
0	X	X	0.000V
1	0	0	0.850V
1	0	1	0.875V
1	1	0	0.950V
1	1	1	0.975V

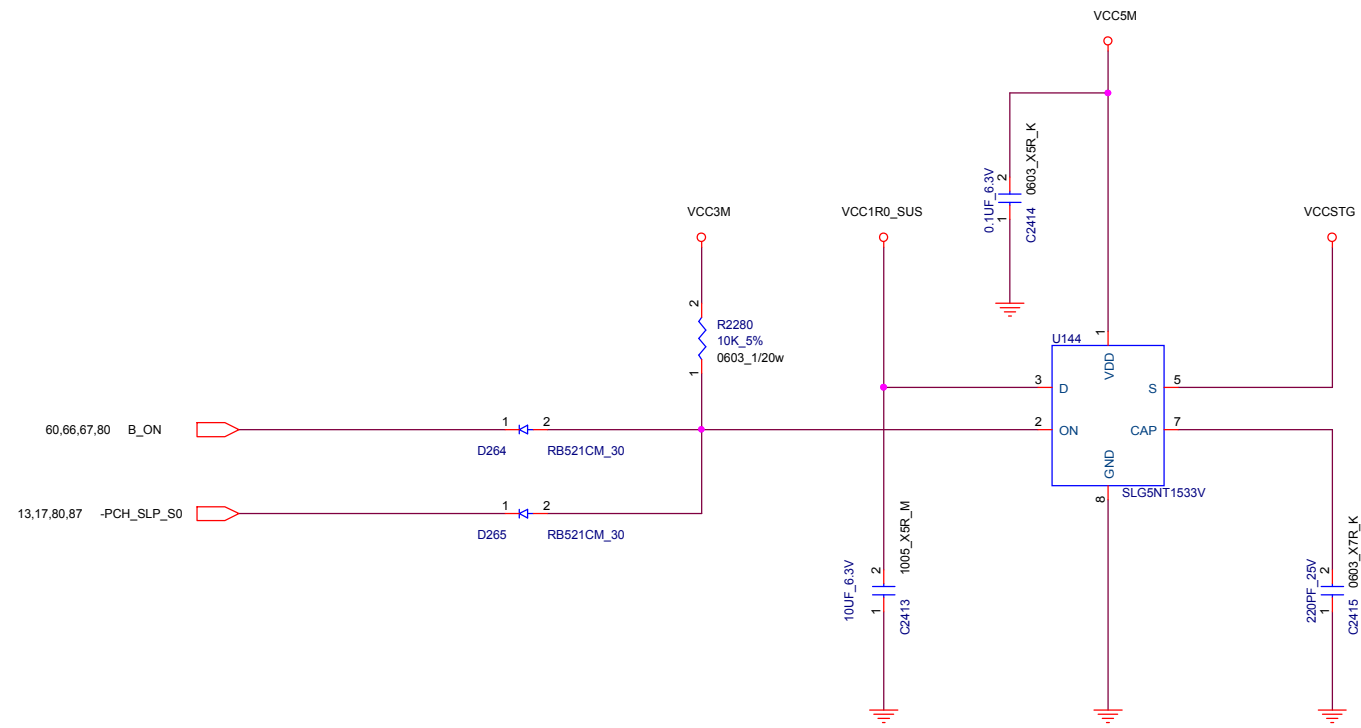
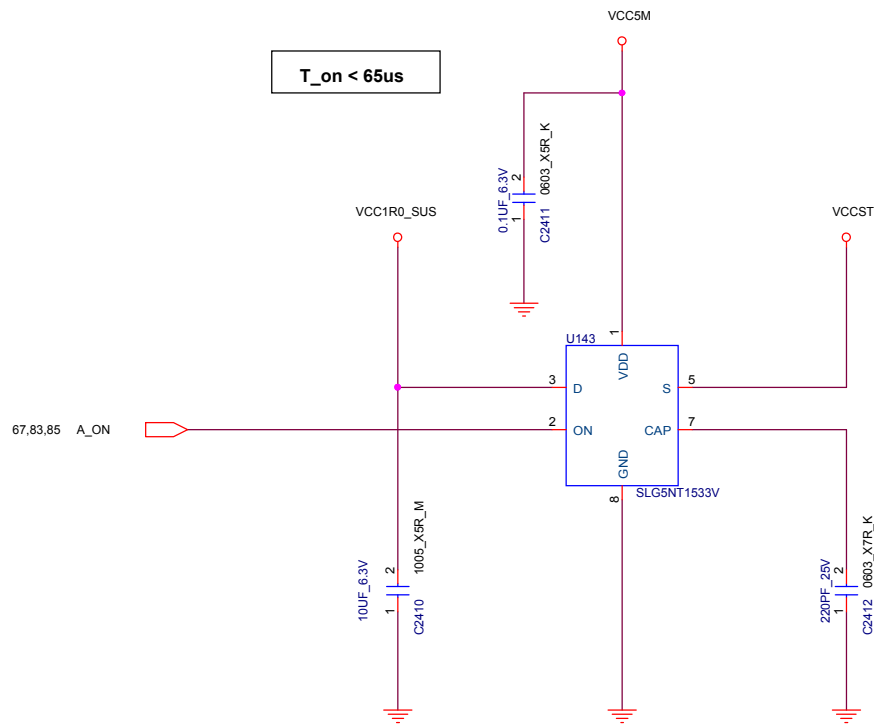
— SLP_S0#

— LOGIC

Note: R2061 should be 0ohm if remote sense is not used.

Differential Lines





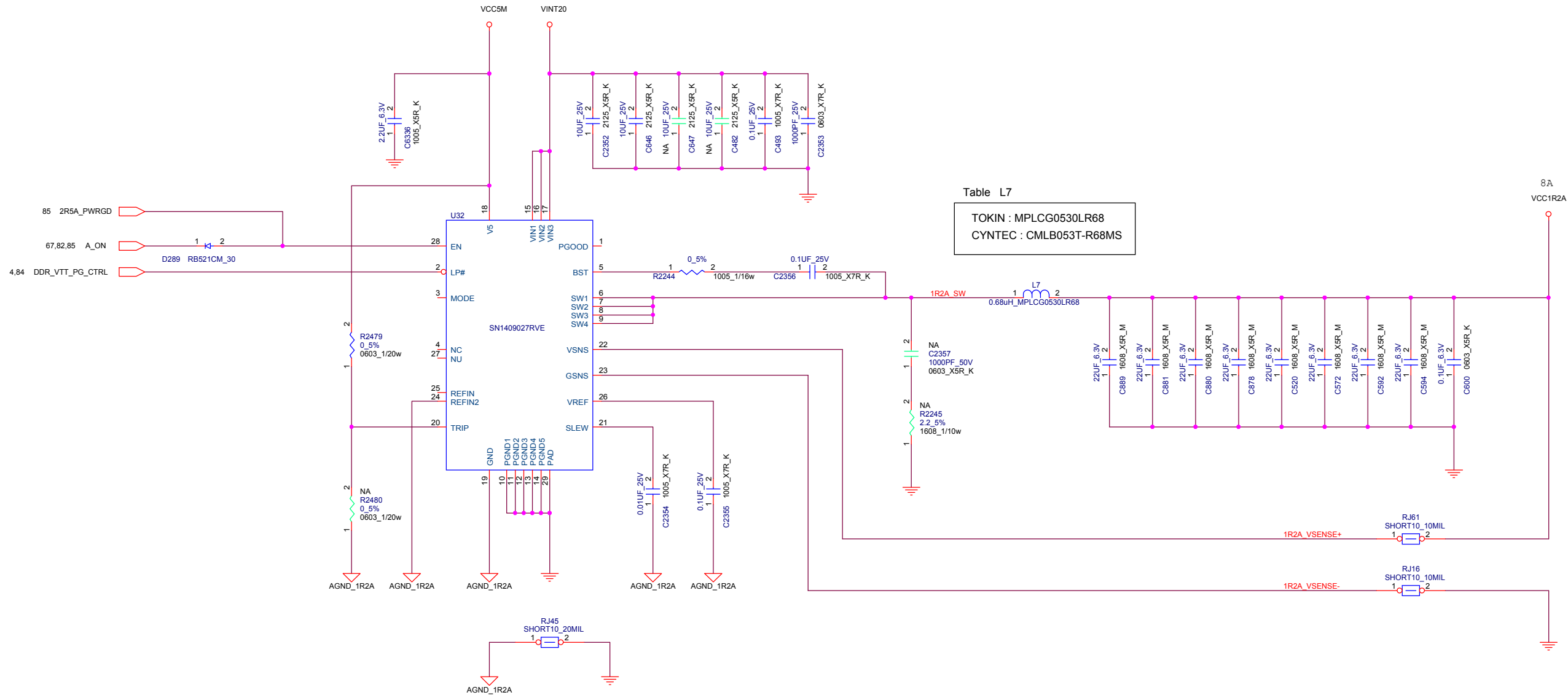


Table L7

TOKIN : MPLCG0530LR68
CYNTEC : CMLB053T-R68MS

TABLE : TPSS1362

REFIN	REFIN2	VOUT
GND	GND	1.05V
Float	GND	1.20V
GND	Float	1.50V
Float	Float	1.35V

← LOGIC

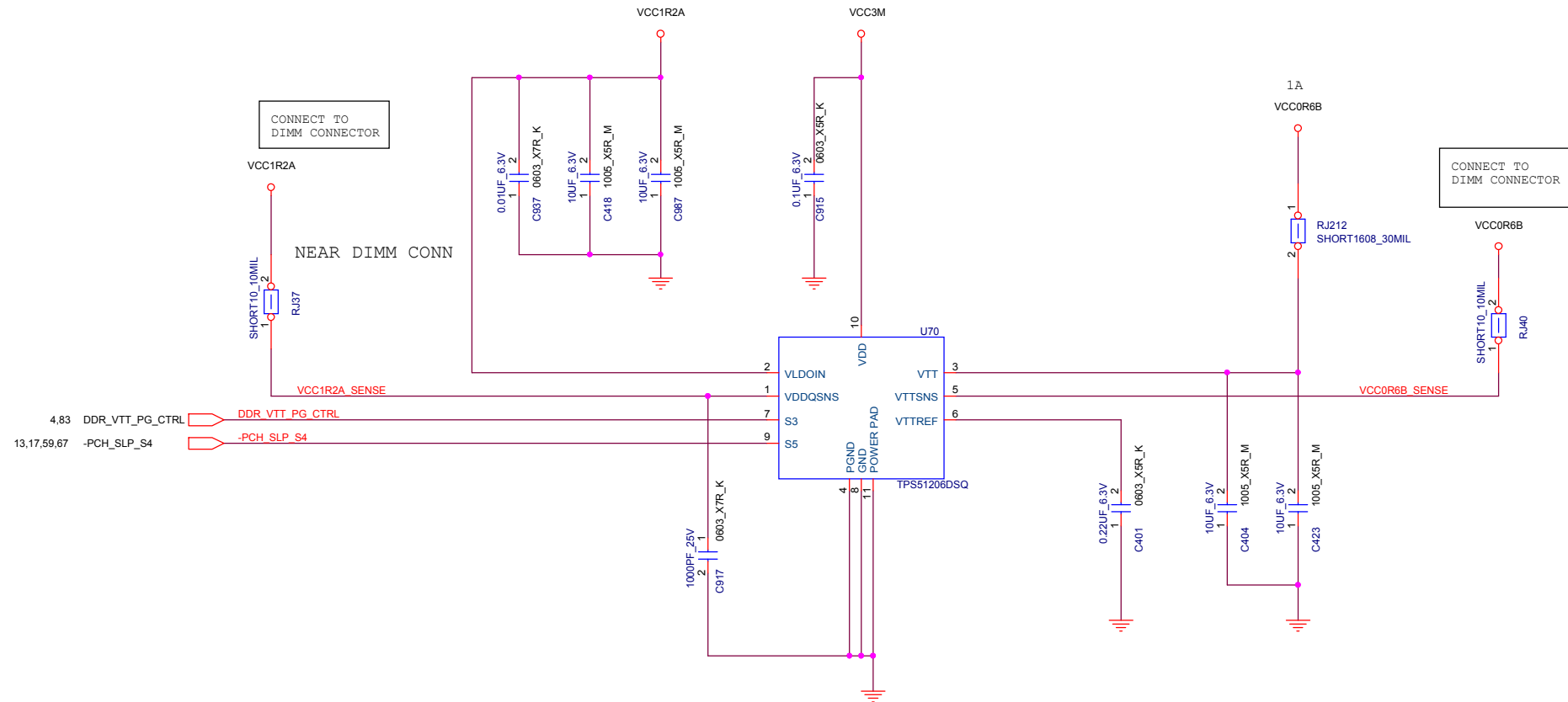
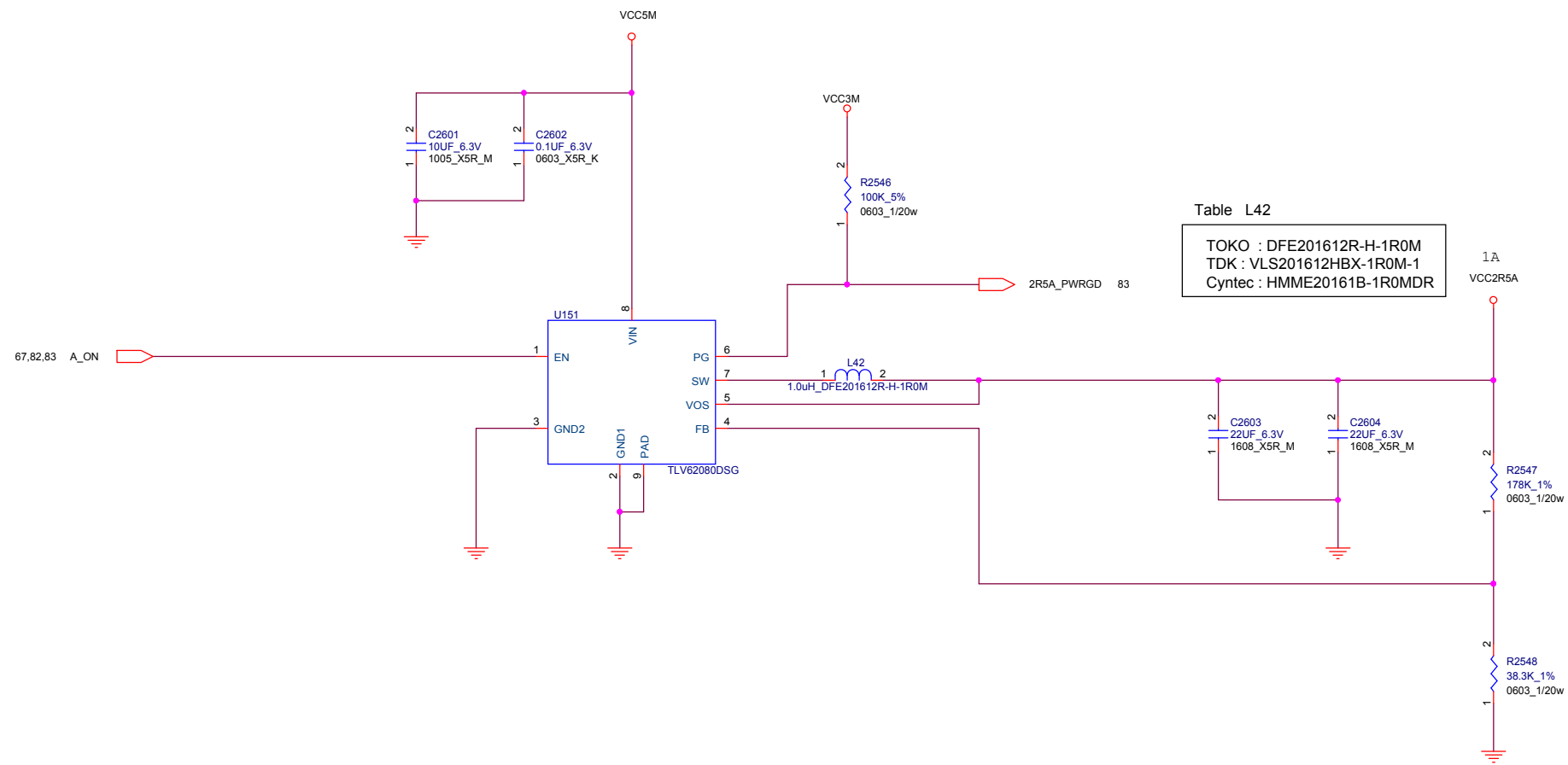


TABLE: TPS51206

S3	S5	VTT	VTTREF
High	High	ON	ON
Low	High	OFF(High-Z)	ON
Low	Low	OFF(Discharge)	OFF(Discharge)





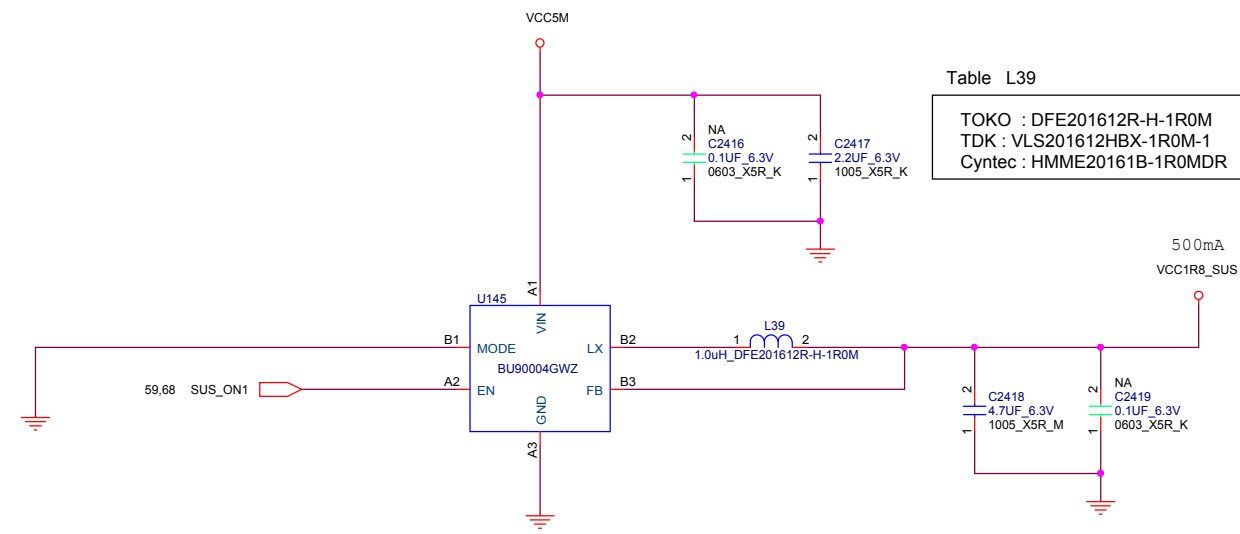


Table L39

TOKO	: DFE201612R-H-1R0M
TDK	: VLS201612HBX-1R0M-1
Cyntec	: HMME20161B-1R0MDR

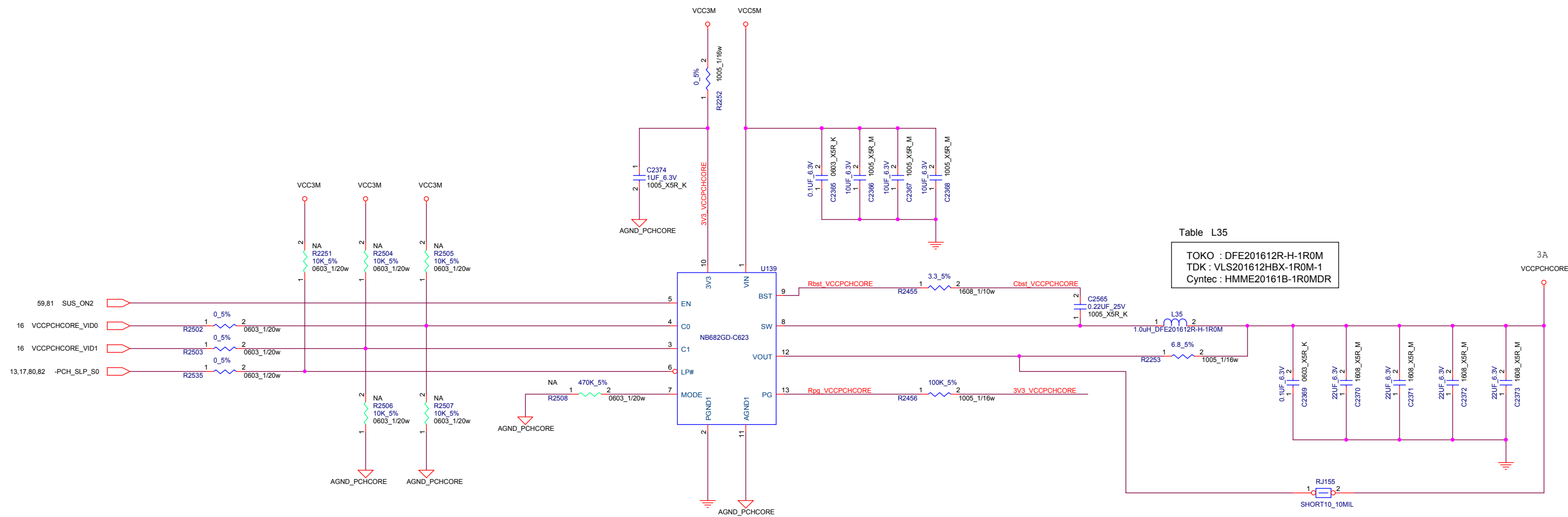


Table L35

TOKO : DFE201612R-H-1R0M
 TDK : VLS201612HBX-1R0M-1
 Cyntec : HMME20161B-1R0MDR

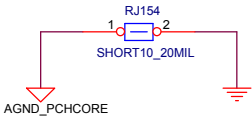
Note: R2253 should be 0ohm if J155 is not short.

TABLE : NB682 MODE M2 (Float)

LP#	C1	C0	VOUT
0	X	X	0.700V
1	0	0	0.850V
1	0	1	0.900V
1	1	0	0.950V
1	1	1	1.000V

← SLP_S0#

← DEFAULT



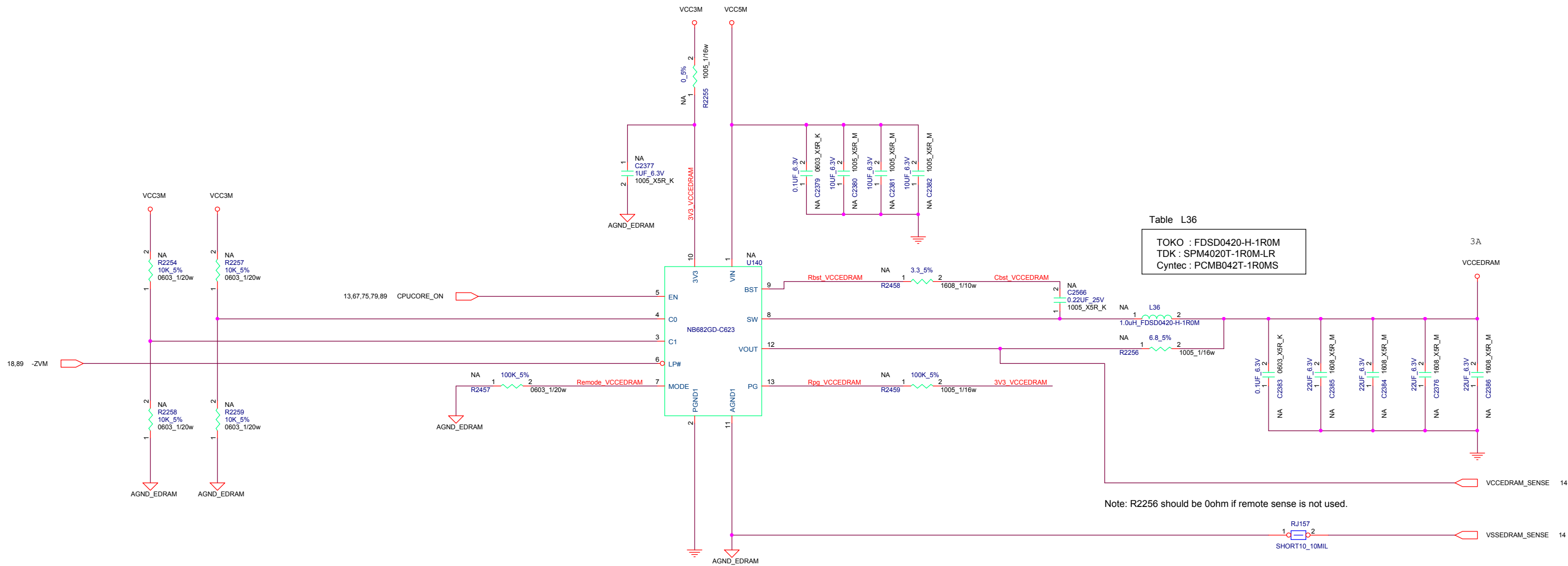


TABLE : NB682 MODE M3 (100K to GND)

LP#	C1	C0	VOUT
0	X	X	0.000V
1	0	0	0.800V
1	0	1	0.950V
1	1	0	1.000V
1	1	1	1.050V

← ZVM#

← LOGIC



Project Name : THP1_SWG_SOVP Title : DC/DC VCCEDRAM(NB682)

Size : C Document Number : Rev : 8.04

Date: Tuesday, December 15, 2015 Sheet : 88 of 99

All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

Switching Frequency	Control Mode	R2120	C2190	C2192
500kHz	D-CAP2	1Kohm	ASM	NO_ASM
400kHz	D-CAP	200Kohm	NO_ASM	ASM
300kHz	D-CAP	100Kohm	NO_ASM	ASM

LOGIC

U124 :

TI SN74LVC1G126DRL

Renesas HD74LV1G126AVSE

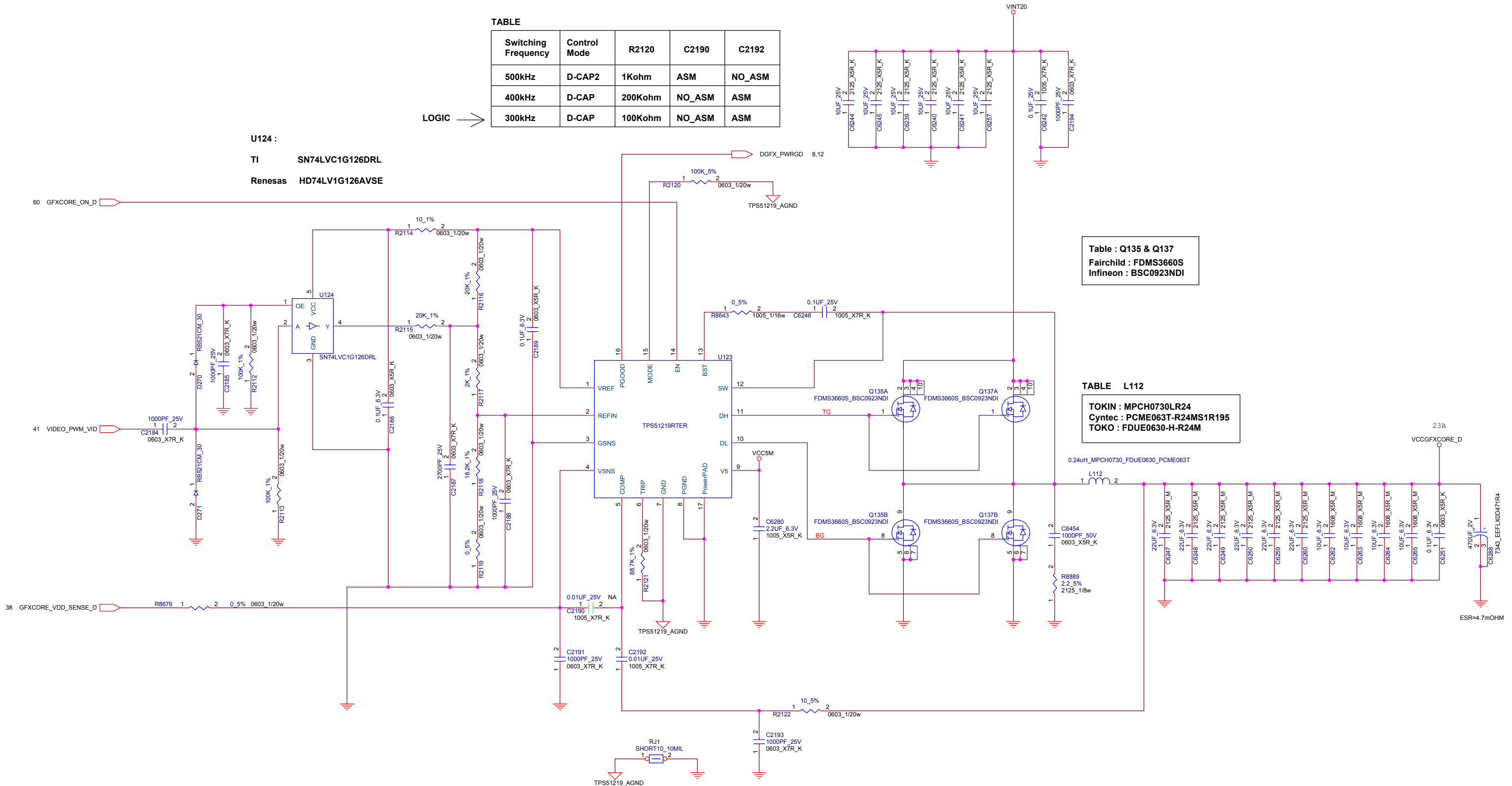


Table : Q135 & Q137
Fairchild : FDMS3660S
Infineon : BSC0923NDI

TABLE L112

TOKIN : MPCH0730LR24
Cyntec : PCME063T-R24MS1R195
TOKO : FDUE0630-H-R24M

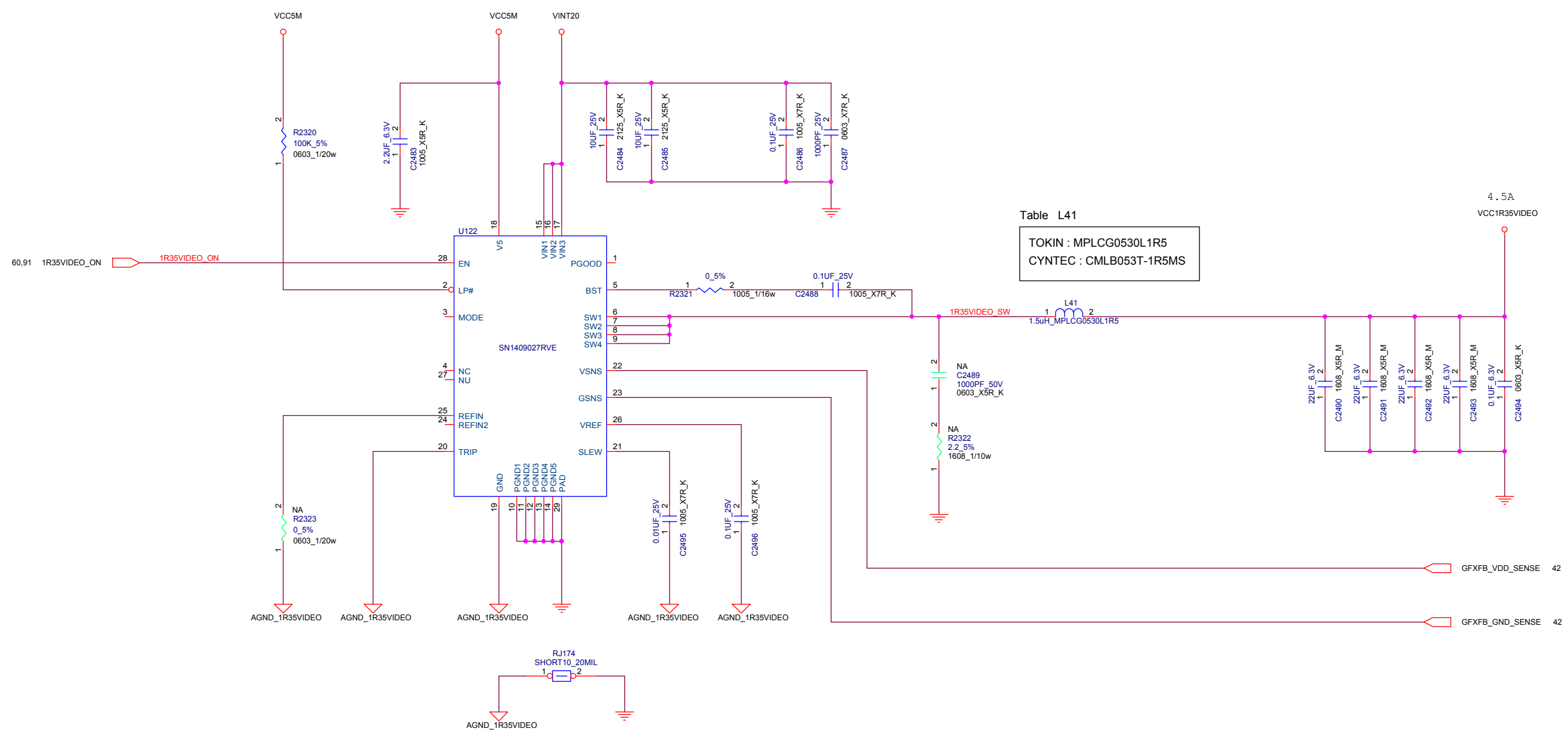
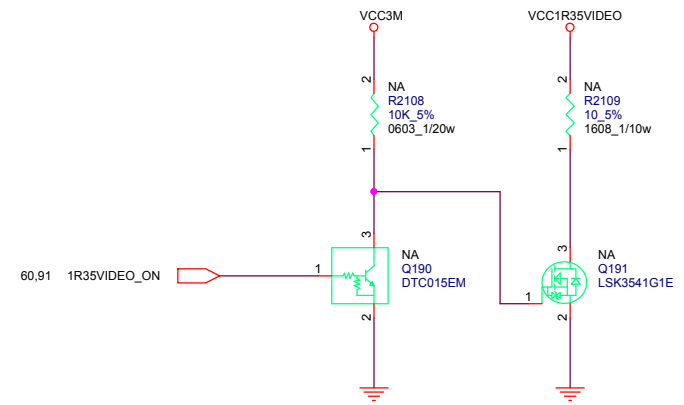


TABLE : TPS51362

REFIN	REFIN2	VOUT
GND	GND	1.05V
Float	GND	1.20V
GND	Float	1.50V
Float	Float	1.35V

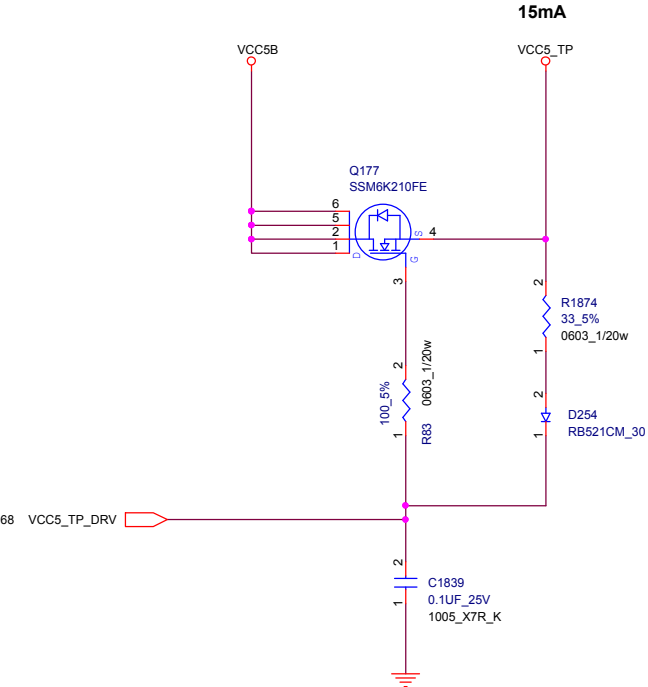
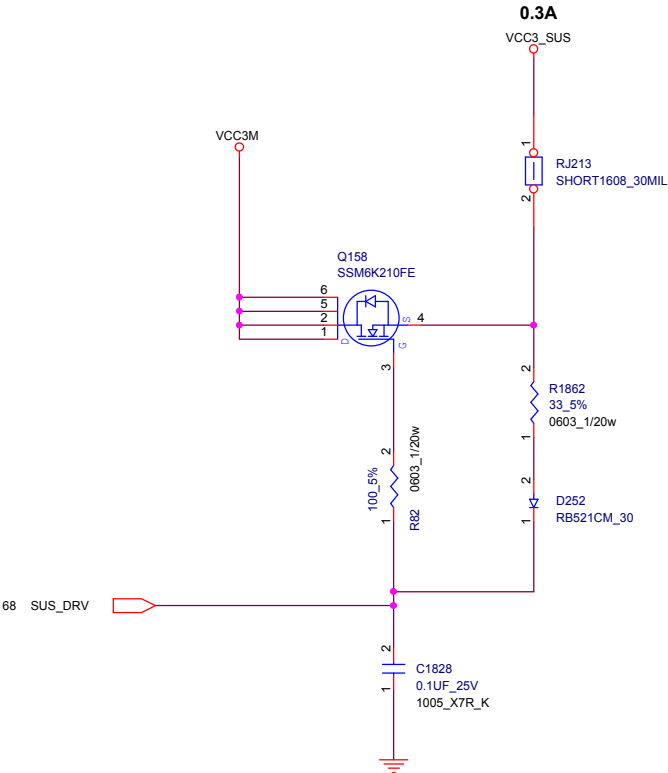
← LOGIC

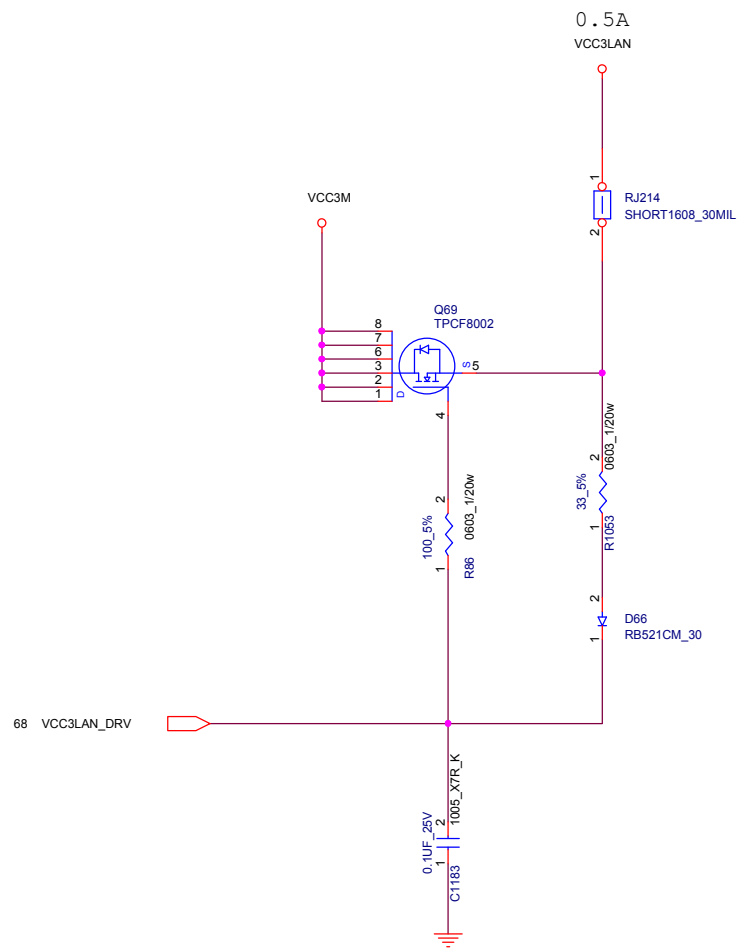


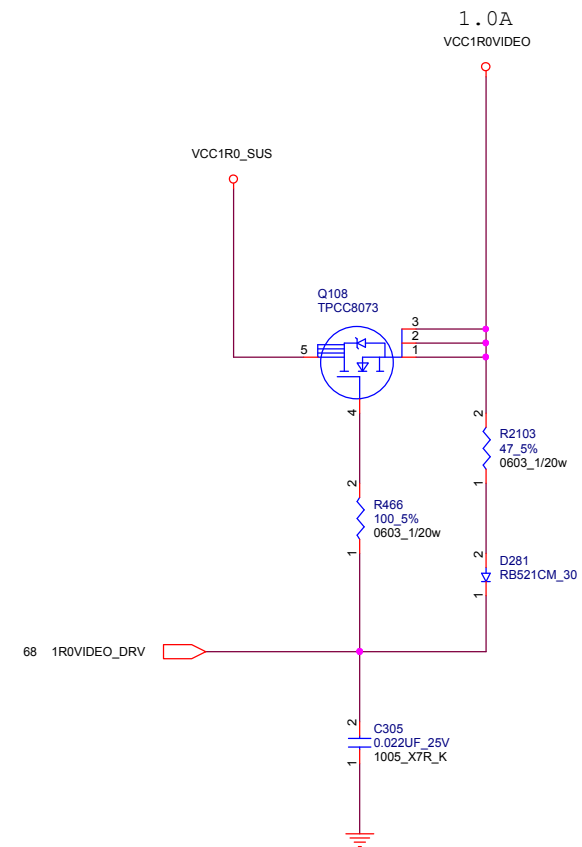
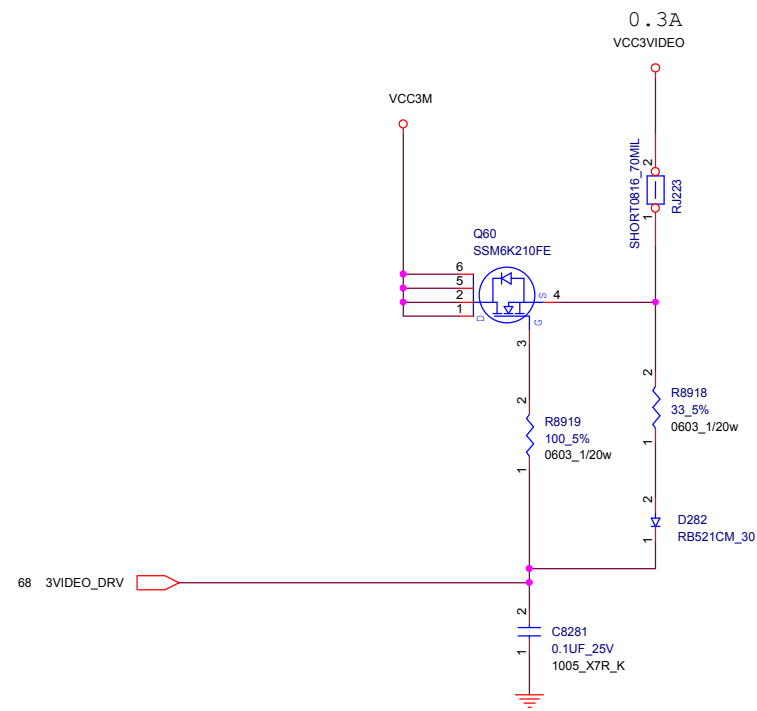
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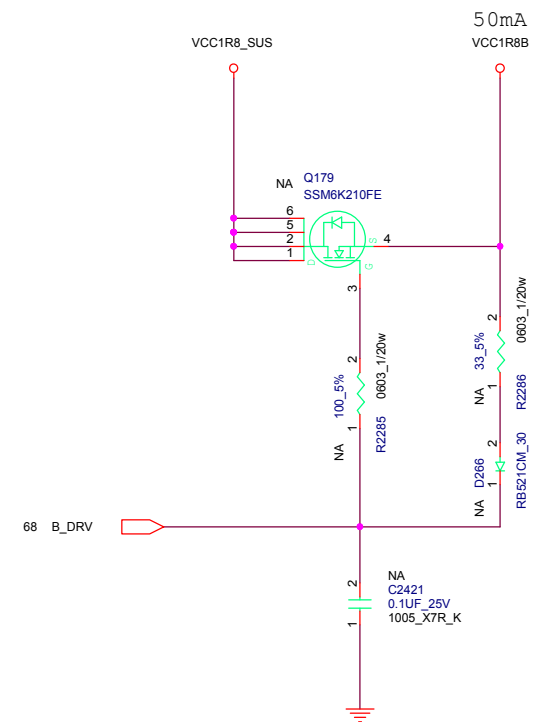
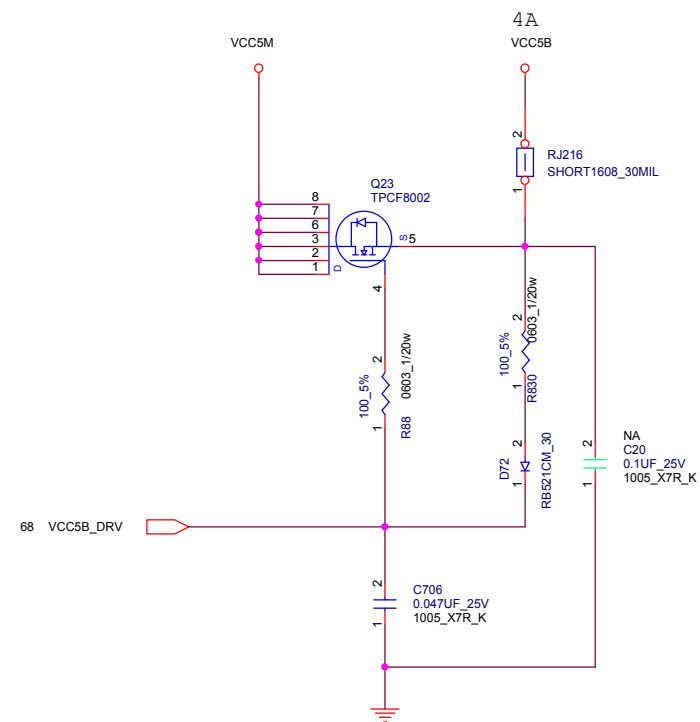
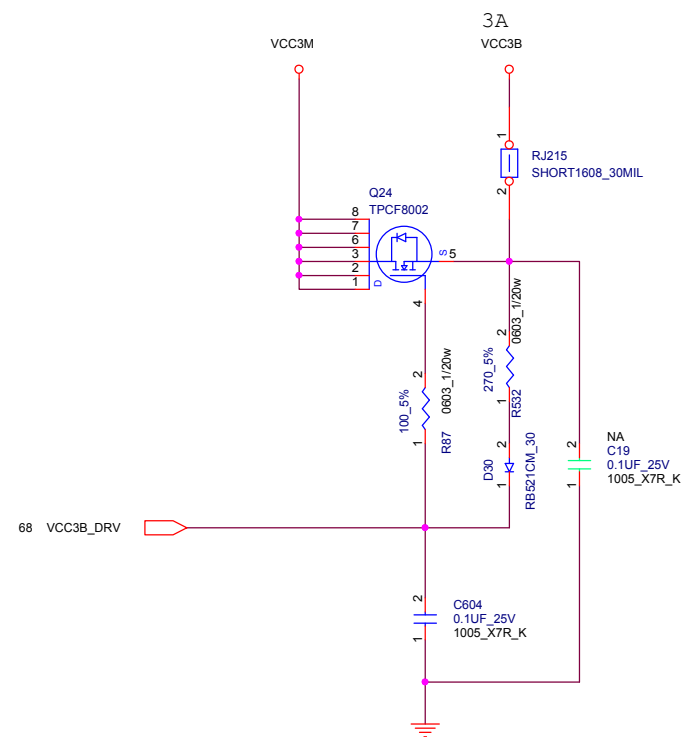


Project Name : THP1_SWG_SOVP		Title : BLANK	
Size : C	Document Number :		Rev : 8.04
Date: Tuesday, December 15, 2015		Sheet :	92 of 99








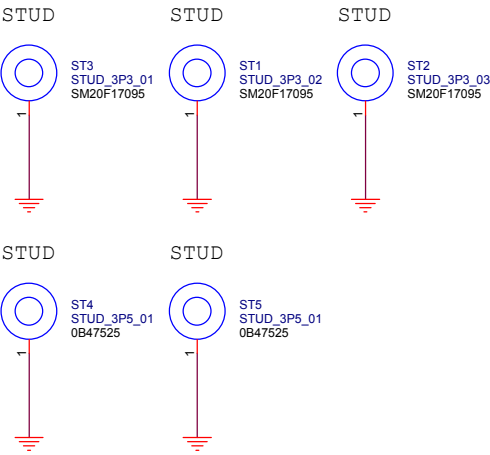
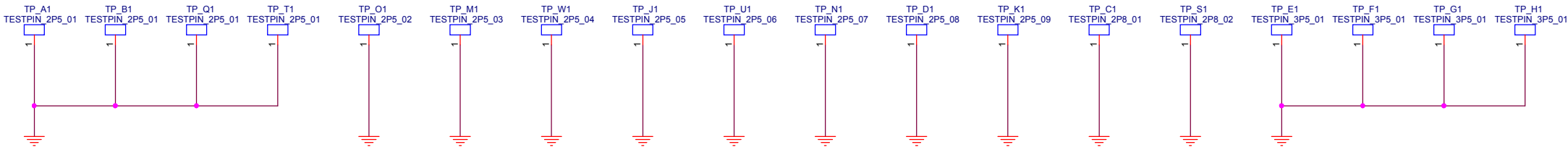


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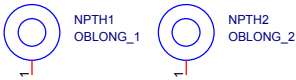
		
Project Name : THP1_SWG_SOVP		Title : BLANK
Size : C	Document Number :	Rev : 8.04
Date: Tuesday, December 15, 2015		Sheet : 98 of 99

PTH FOR SCREW HOLE

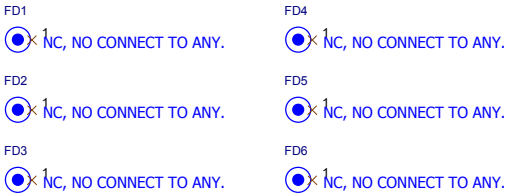
Value	Hole Dia	Pad Dia		QTY
		TOP	BOTTOM	
TESTPIN_2P5_01	2.5	6.5	6.5	4
TESTPIN_2P5_02	2.5	6.6	6.6	1
TESTPIN_2P5_03	2.5	6.6	0	1
TESTPIN_2P5_04	2.5	6.5	9.1	1
TESTPIN_2P5_05	2.5	6.5	7	1
TESTPIN_2P5_06	2.5	6.5	6	1
TESTPIN_2P5_07	2.5	6.6	7	1
TESTPIN_2P5_08	2.5	7	7	1
TESTPIN_2P5_09	2.5	6.5	0	1
TESTPIN_2P8_01	2.8	7	6.5	1
TESTPIN_2P8_02	2.8	7	6.6	1
TESTPIN_3P5_01	3.5	7	6.5	4
STUD_3P3_01 (SM20F17095)	3.3	6.5	6.5	1
STUD_3P3_02 (SM20F17095)	3.3	6.6	6.5	1
STUD_3P3_03 (SM20F17095)	3.3	6.6	6.6	1
STUD_3P5_01 (0B47525)	3.5	7	7	2



NPTH



FID
Board Area



FID
Component Area

